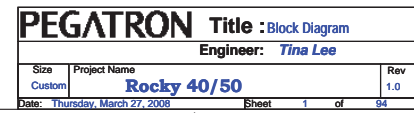
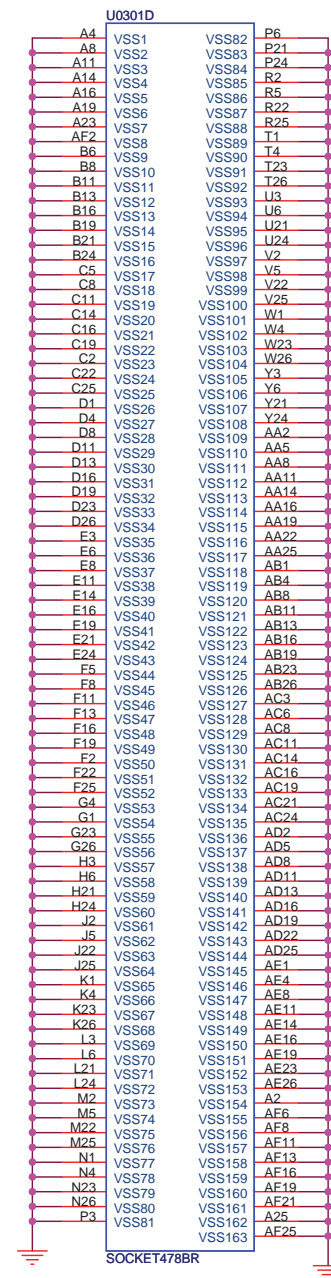


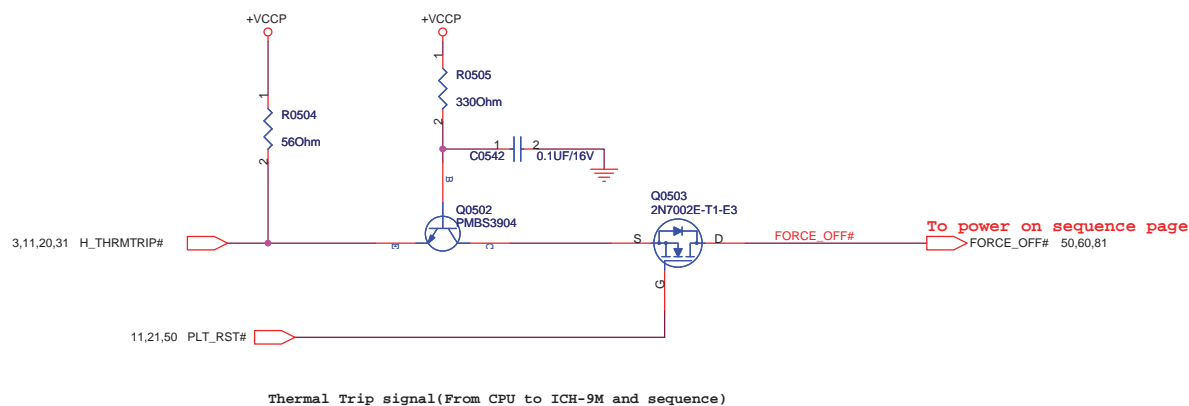
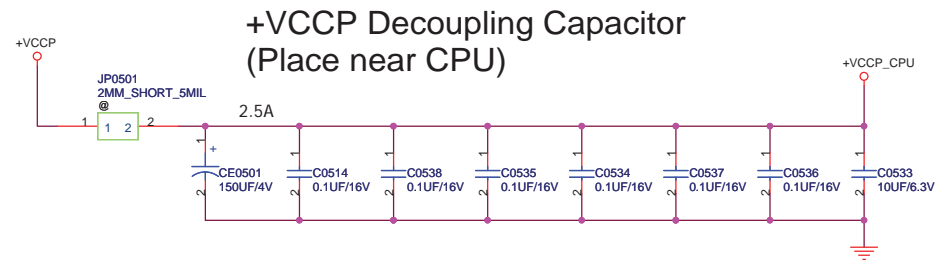
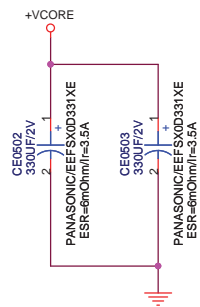
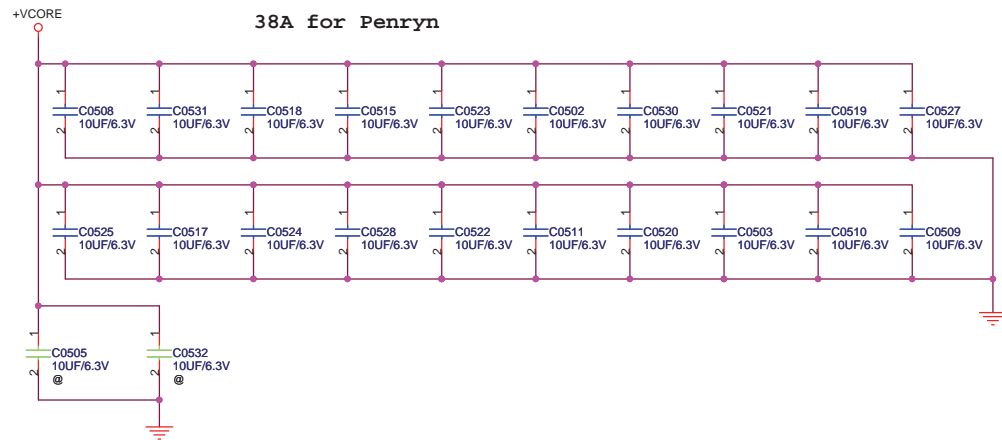
**WWW.AliSaler.Com**











<b>PEGATRON</b>		<b>Title : CPU CAPS</b>	
		<b>Engineer: Tina Lee</b>	
Size Custom	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Thursday, March 27, 2008		Sheet 5 of 94	

5	4	3	2	1
D				
C				
B				
A				

PEGATRON Title :		
Engineer: Tina Lee		
Size A4	Project Name Rocky 40/50	Rev 1.0
Date: Friday, March 14, 2008	Sheet 6	of 94

+3VSO +3VS 3,8,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,56,57,58,59,61,91,92  
+1.8VSO +1.8V 8,9,11,13,83,91  
M\_VREF\_MCH M\_VREF\_MCH 8,9,11

SMBus Slave Address:A0H

temp\_5886\_t101  
(12G025M22000LV with 12G025C2200WLV  
co-lay symbol)

SMBus Slave Address: A0H

Place near SO-DIMM\_0

Layout Note: Place these caps near SO DIMM 0

Layout Note: Place these Caps near SO DIMM 0

PLACE NEAR SO-DIMM\_0 / SO-DIMM\_1

Layout Note: Place these caps near SO DIMM 0

VREF -> 10/10 mils




SO-DIMM 0 is placed nearer the  
GMCH than SO-DIMM 1

PEGATRON Title DDR2 SO-DIMM\_0

Engineer: Tina Lee

Size	Project Name	Rev
Custom	Rocky 40/50	1.0
Date: Thursday, March 27, 2008	Sheet 7 of 94	



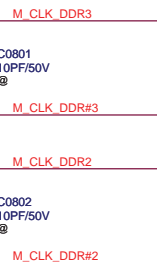
+3VS  +3VS 3,7,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,56,57,58,59,61,91,92  
+1.8V  +1.8V 7,9,11,13,83,91  
M\_VREF\_MCH  M\_VREF\_MCH 7,9,11

temp\_5886\_t102  
(12G025032005LV with 12G025022004LV  
CO-LAY symbol)

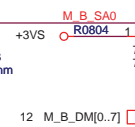
9,12 M\_B\_A[0..14]

M\_B\_DQ[0..63] 12

SMBus Slave Address:A4H



Place near SO-DIMM\_1

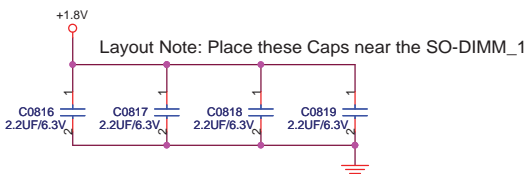


12 M\_B\_DM[0..7]

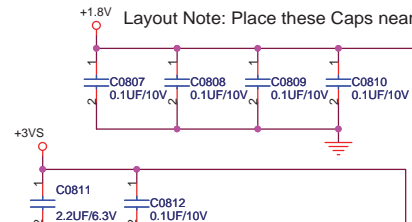
12 M\_B\_DQS[0..7]

12 M\_B\_DQS#0[0..7]

DDR2\_DIMM\_200P

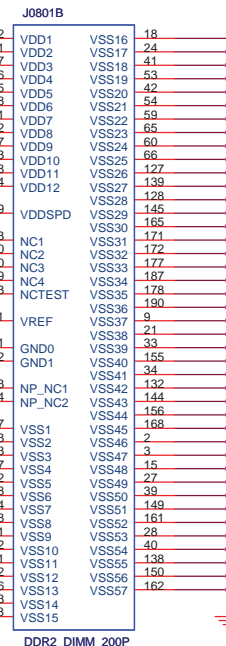


Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these Caps near SO DIMM 1





VREF -> 10/10 mils

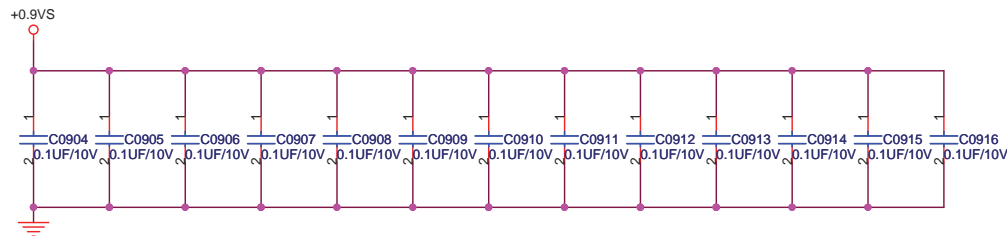
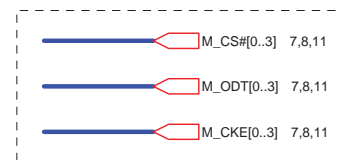
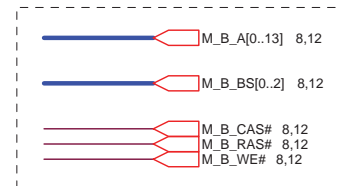
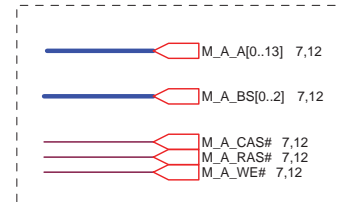
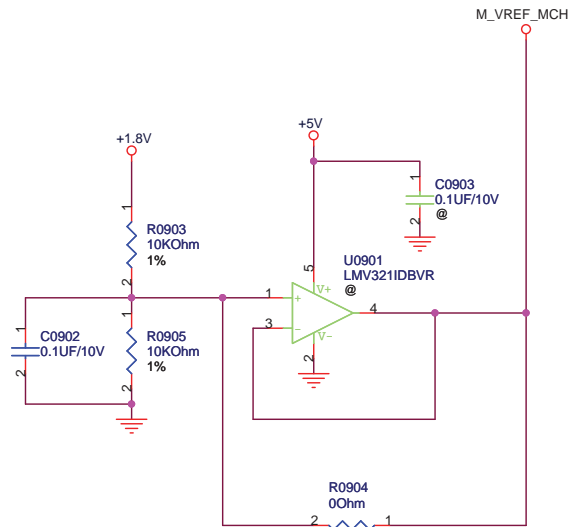


PEGATRON Title :DDR2 SO-DIMM\_1  
Engineer: Tina Lee

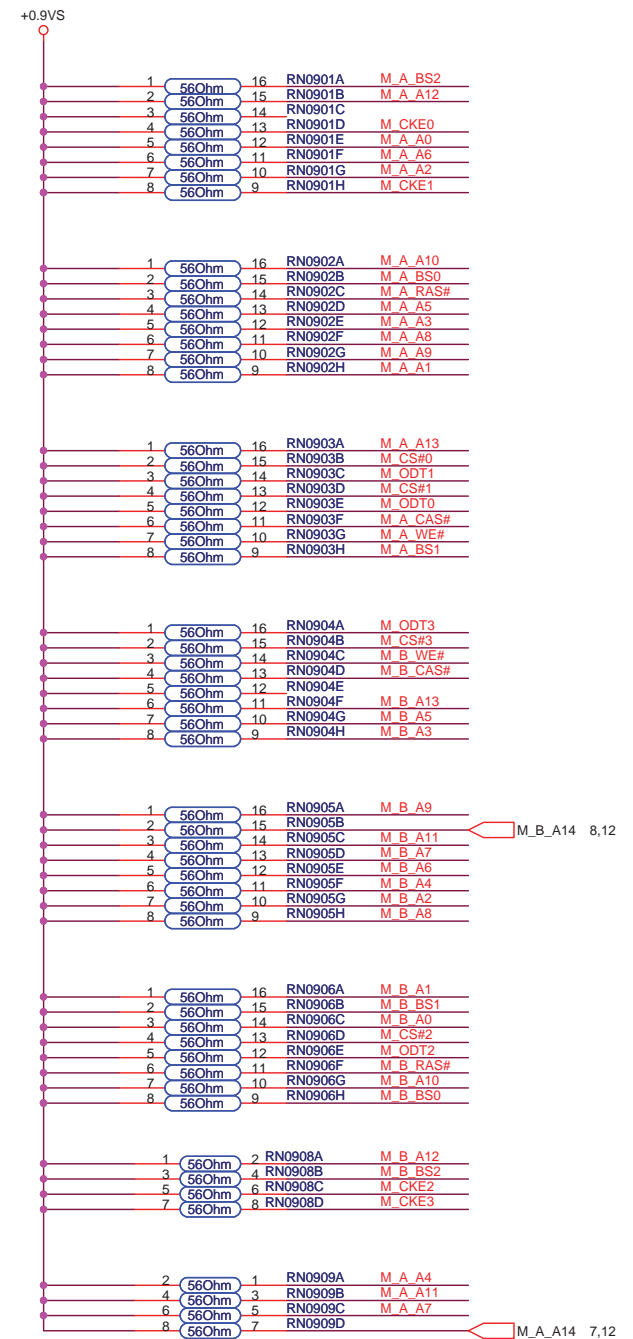
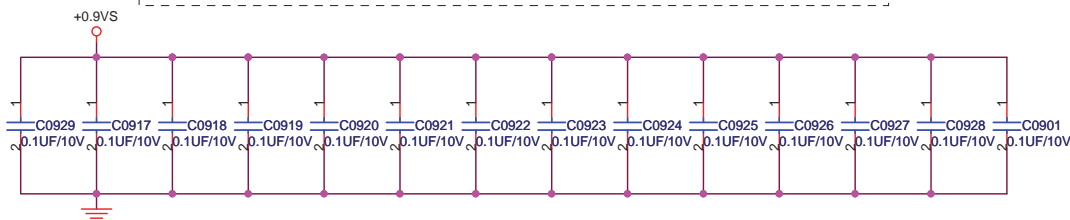
Size	Project Name	Rev
Custom	Rocky 40/50	1.0
Date: Thursday, March 27, 2008	Sheet 8 of 94	



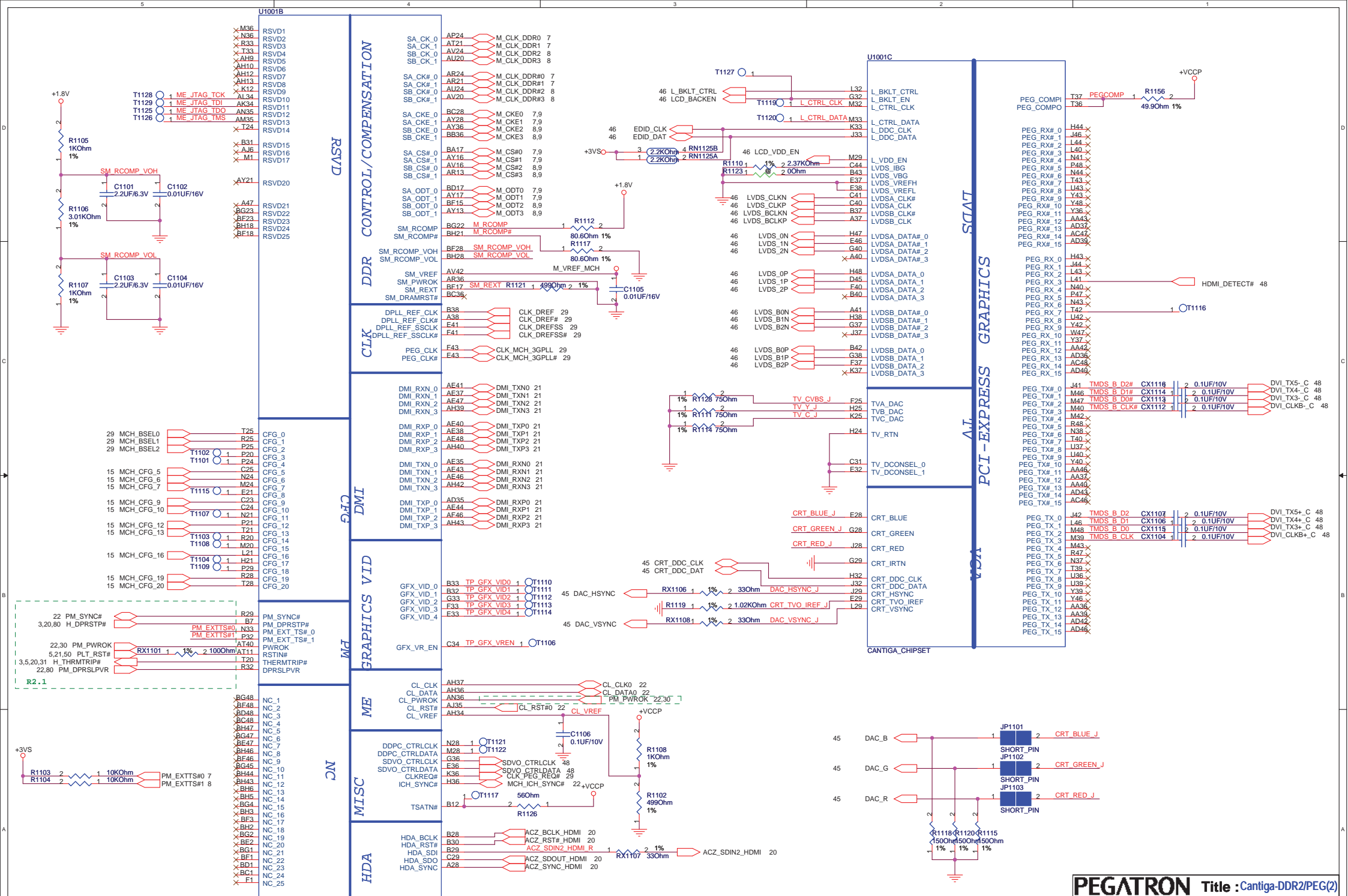
+5V  +5V 44,56,57,91  
 +1.8V  +1.8V 7,8,11,13,83,91  
 M\_VREF\_MCH  M\_VREF\_MCH 7,8,11  
 +0.9VS  +0.9VS 83

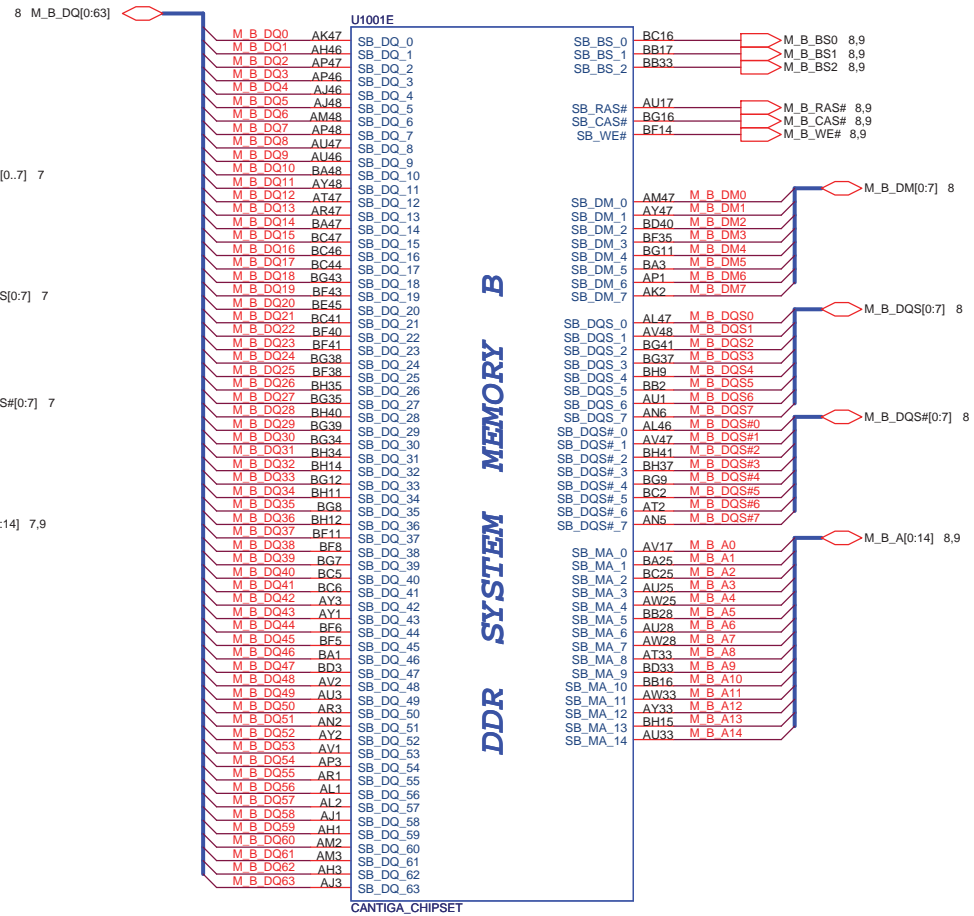
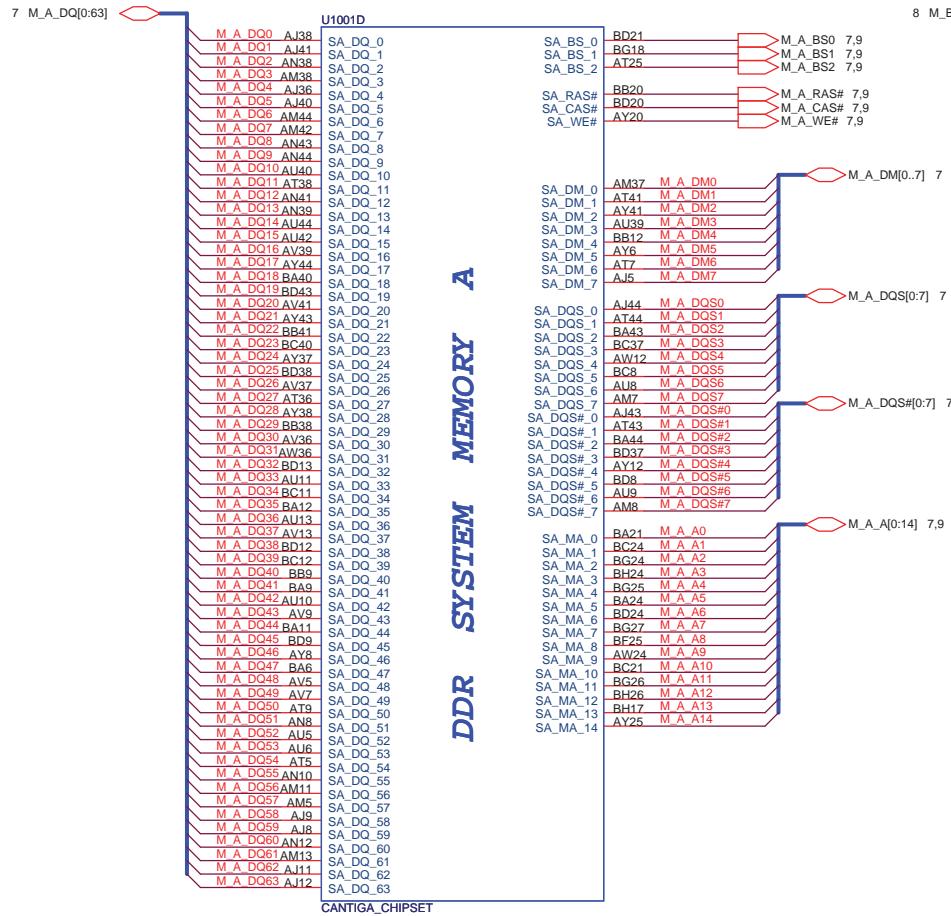


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





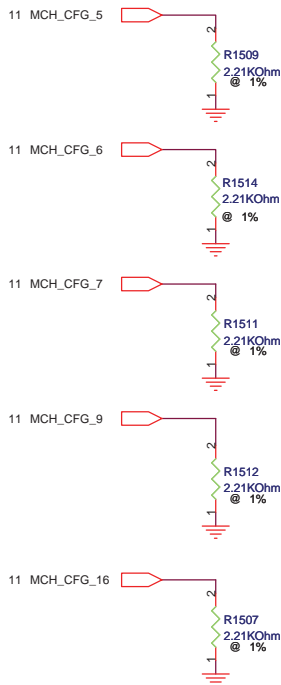












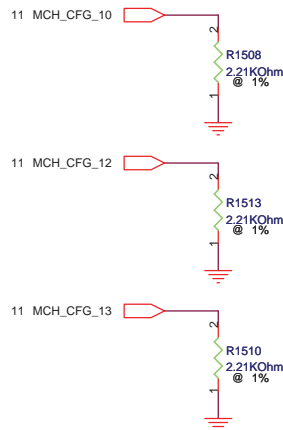
**CFG5 : DMI STRAP**  
**HIGH = DMI X 4 (Default)**  
**LOW = DMI X 2**

**CFG6 : Integrated TPM Host Interface**  
**HIGH = iTPM disable (Default)**  
**LOW = iTPM enable**

**CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite**  
**HIGH = With confidentiality (Default)**  
**LOW = Without confidentiality**

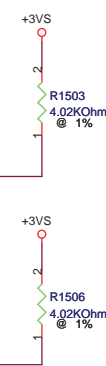
**CFG9 : PCIE GRAPHIC LANE**  
**LOW = Reverse Lanes**  
**HIGH = Normal Operation (Default)**

**CFG16 : FSB Dynamic ODT**  
**HIGH = Enable (Default)**  
**LOW = Disable**



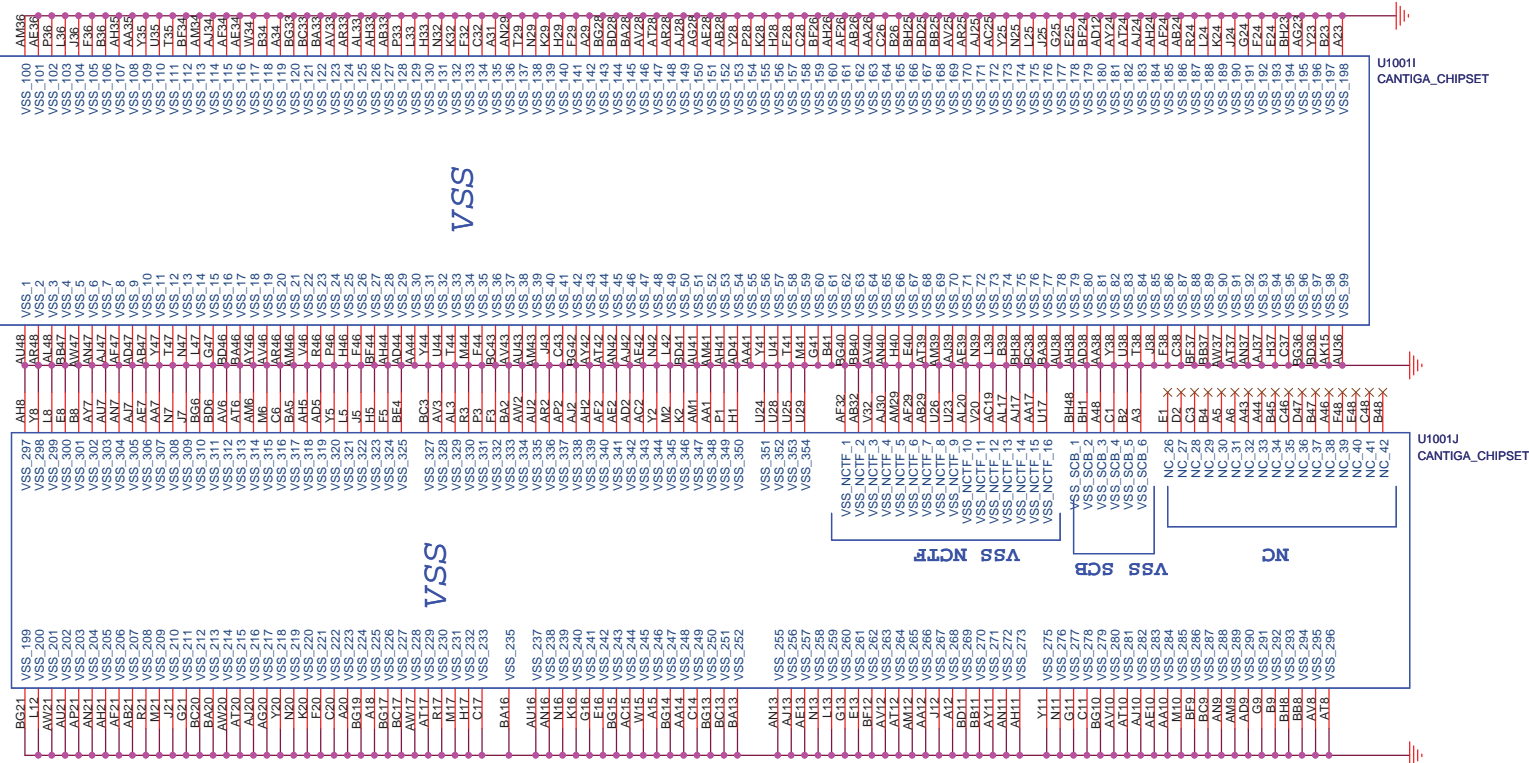
**CFG10 : PCIe Loopback**  
**HIGH = Disable (Default)**  
**LOW = Enable**

**CFG [13:12] : XOR/ALL-Z**  
**00 = Reserved**  
**01 = XOR Mode Enabled**  
**10 = All-Z Mode Enabled**  
**11 = Normal Operation (Default)**



**CFG19 : DMI Lane Reversal**  
**LOW = NORMAL (default)**  
**HIGH = Reverse Lanes**

**CFG20 : SDVO/PCIE CONCURRENT MODE**  
**LOW = ONLY SDVO or PCIE is Operational (Default)**  
**HIGH = SDVO and PCIE are operating simultaneously via the PEG port**





5	4	3	2	1
D				
C				
B				
A				

PEGATRON			Title : ***	
			Engineer: Tina Lee	
Size	Project Name			Rev
A4	Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	16 of 94

5	4	3	2	1
D				
C				
B				
A				

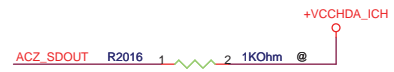
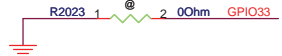
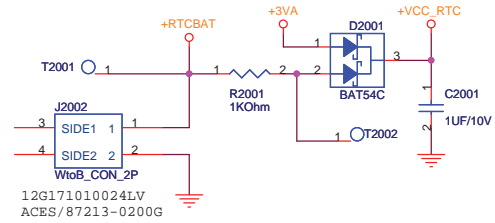
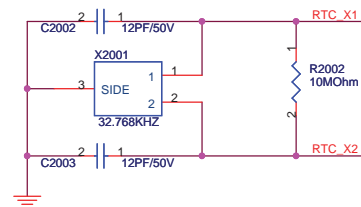
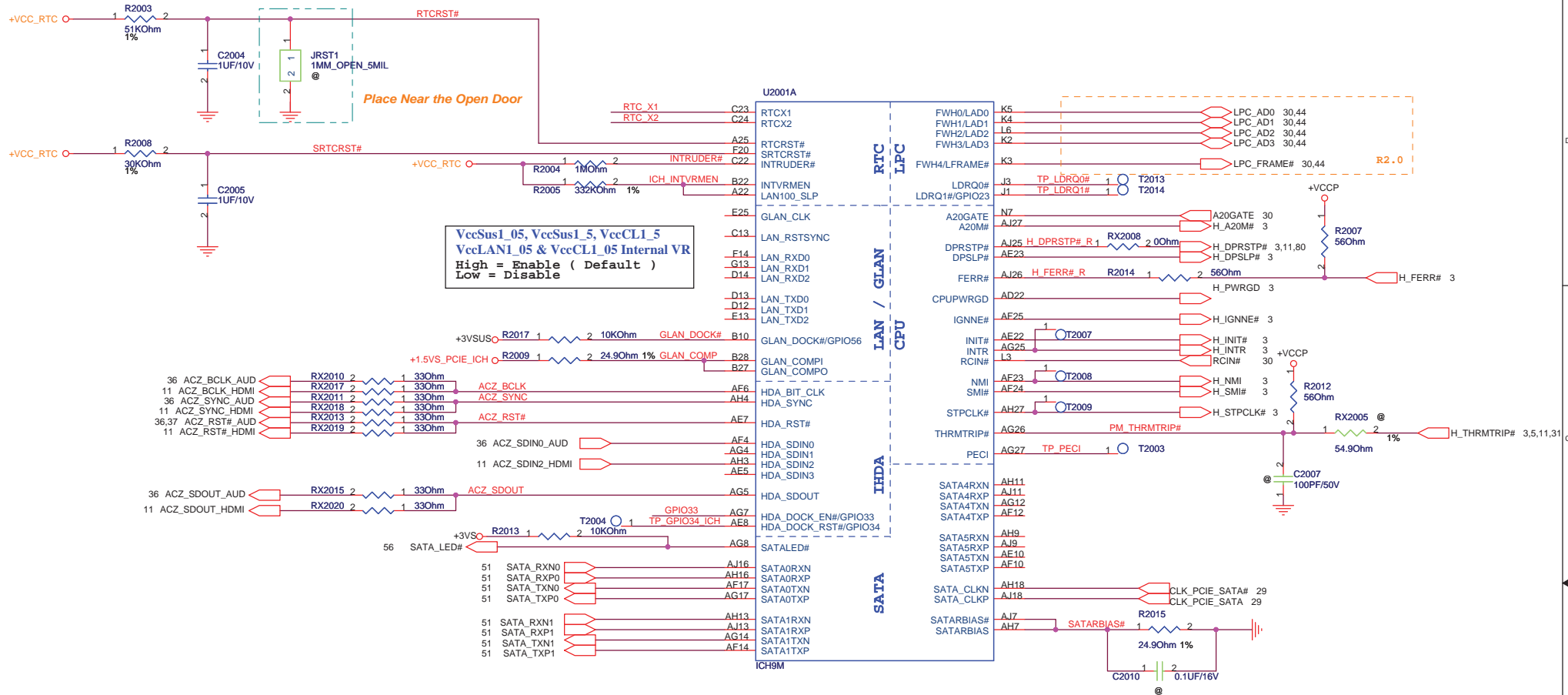
PEGATRON		Title : ***	
		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	17 of 94



PEGATRON		Title : ***	
		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	18 of 94

5	4	3	2	1
D				
C				
B				
A				

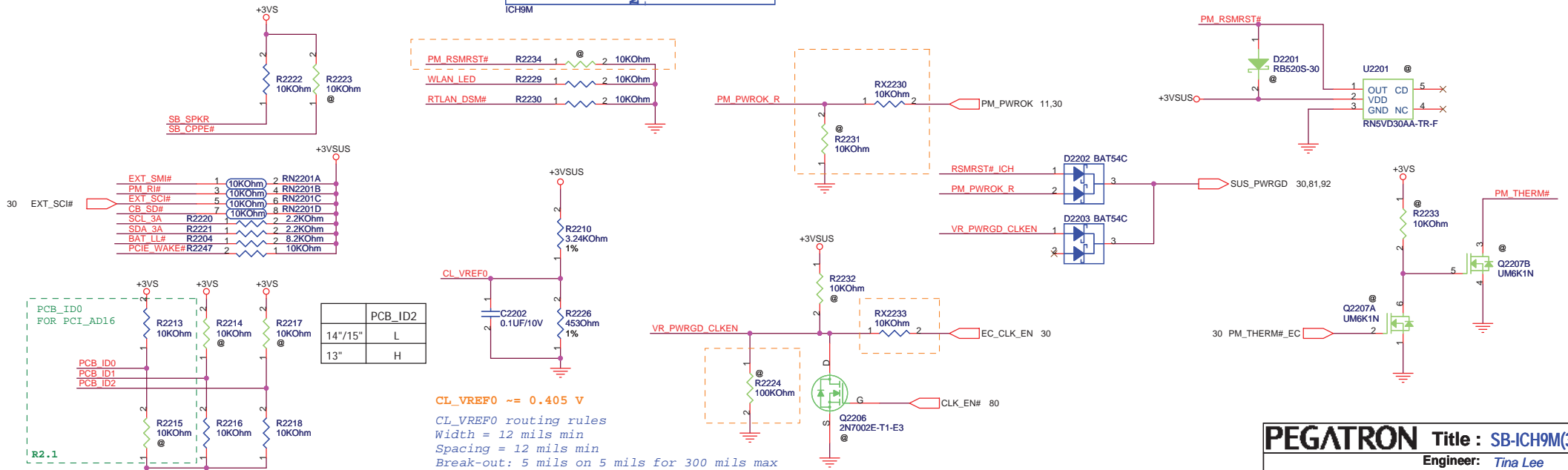
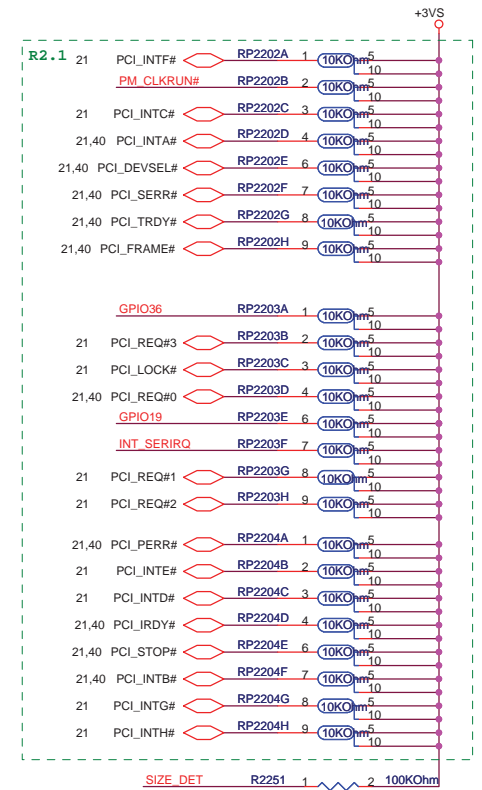
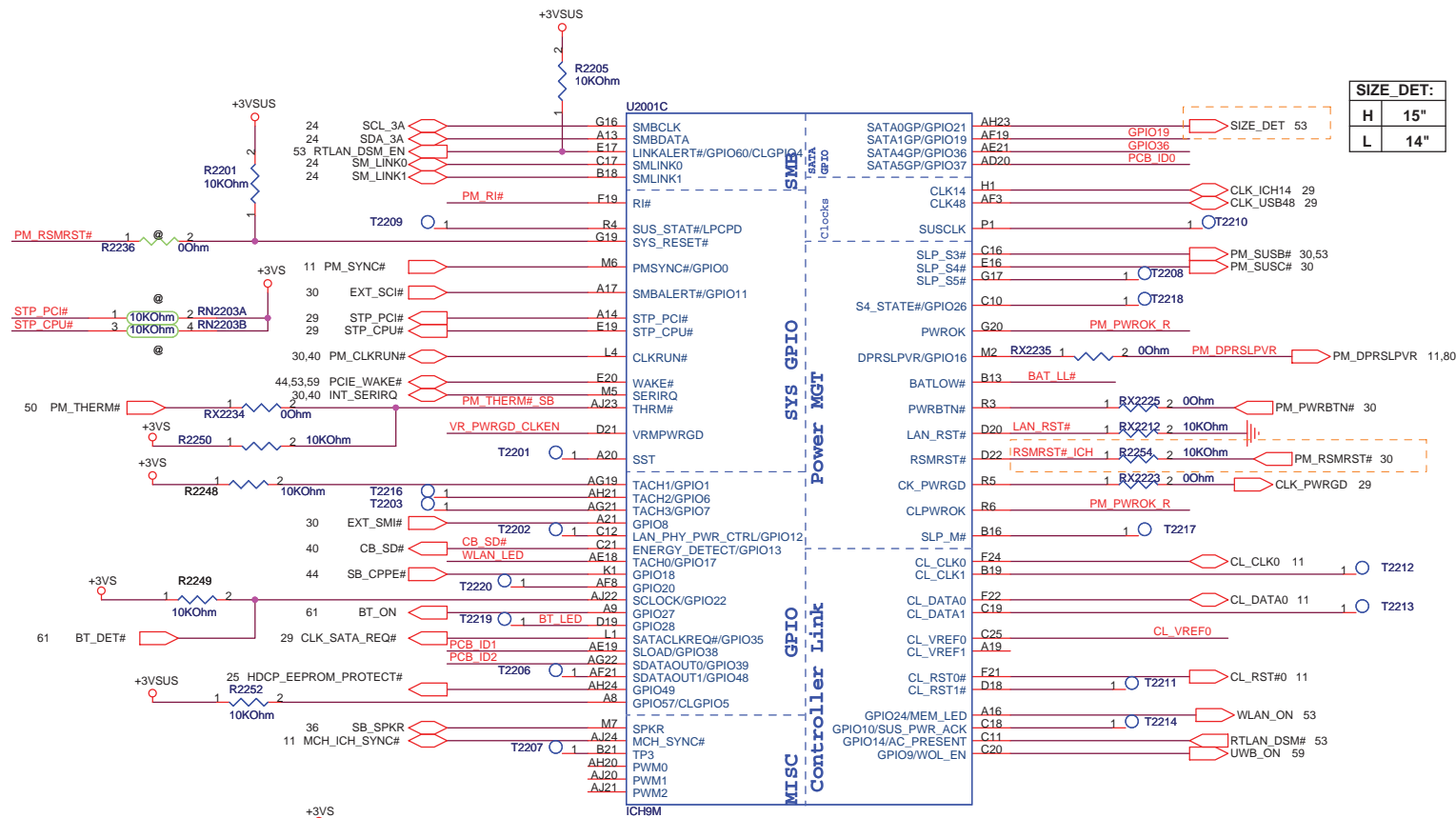
PEGATRON		Title : ***	
		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	19 of 94



[ICH\_TP3, ACZ\_SDOUT] : XOR Chain Entrance Strap

00 = Reserved  
 01 = Enter XOR Chain  
 10 = Normal Operation (Default)  
 11 = Set PCIe Port Config Bit 1

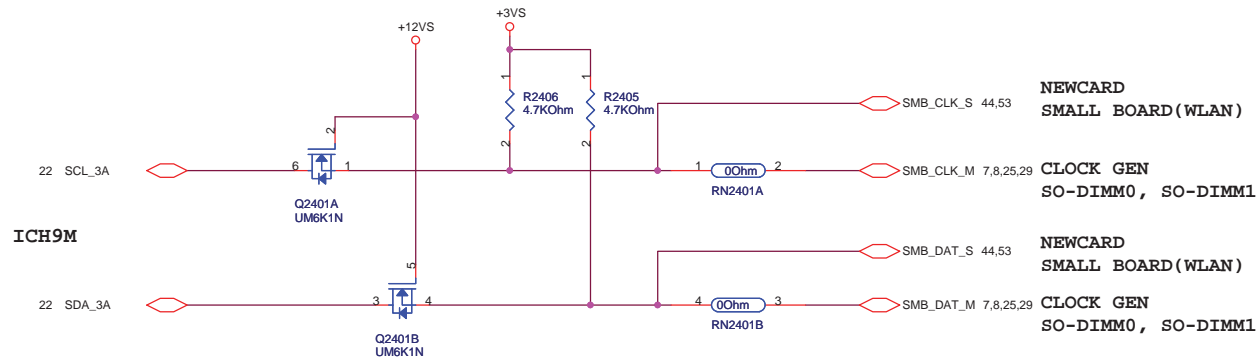




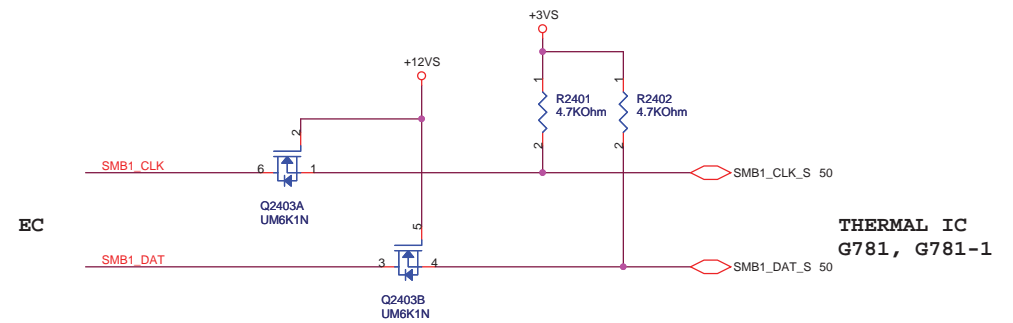
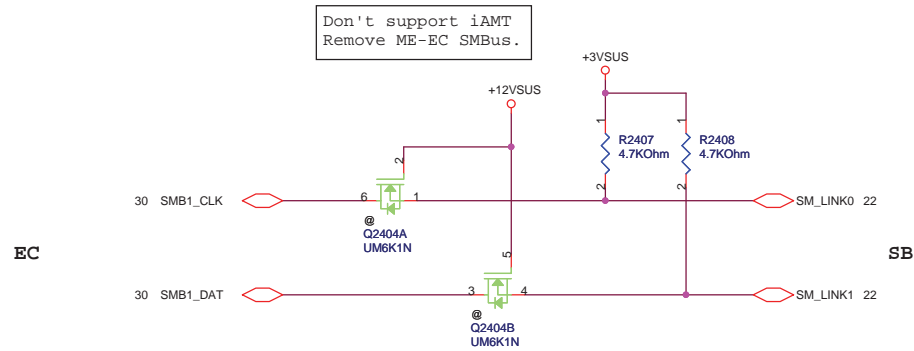


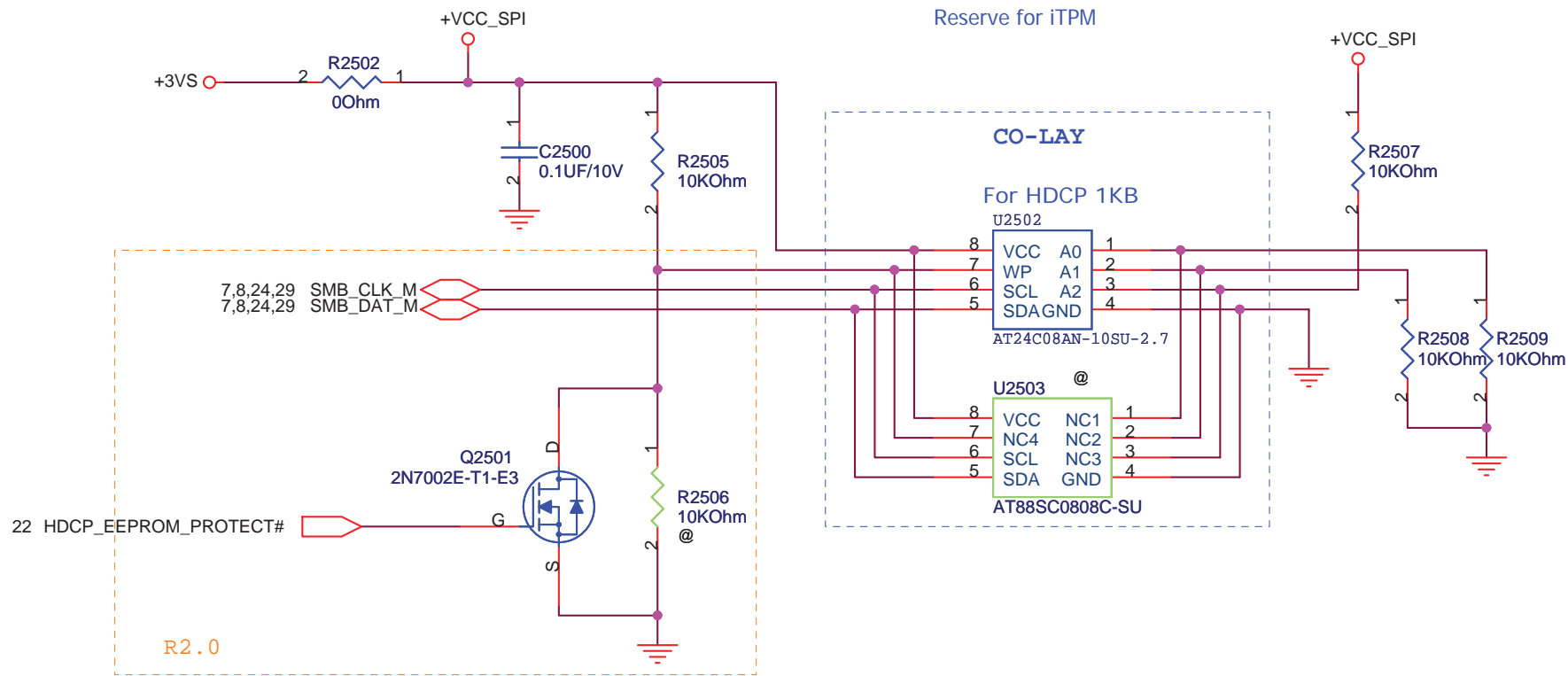
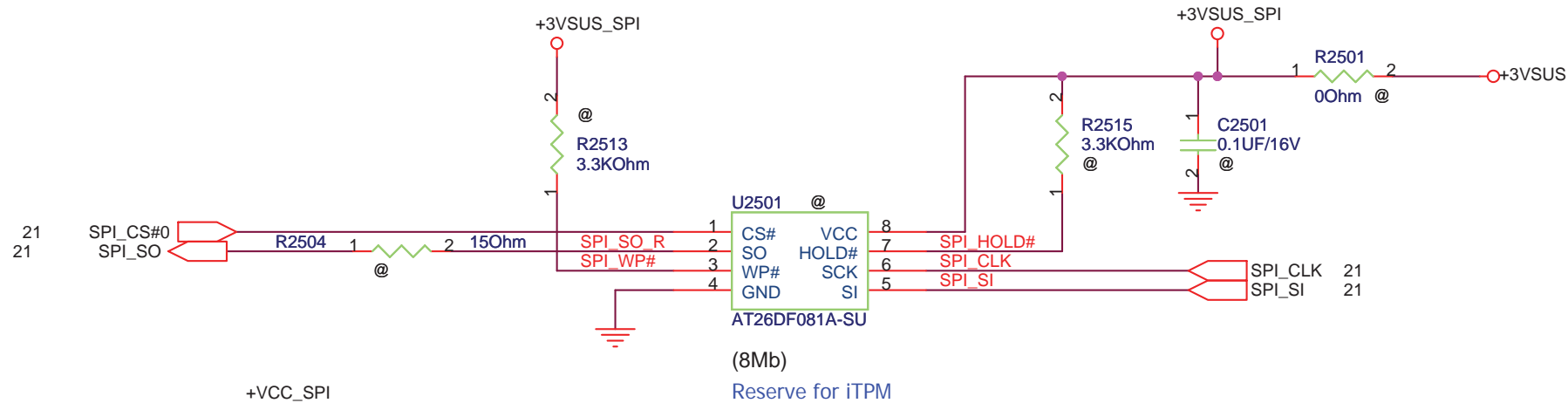


# ICH9-M



# EC





U2502-AT24C08A :  
Stuff : R2506 ; U2502 ; R2507 ; R2508 ; R2509  
Nostuff : R2505

U2503-AT88SC0808C :  
Stuff : U2503  
Nostuff : R2505 ; R2506 ; R2507 ; R2508 ; R2509

<b>PEGATRON</b>			Title : <b>SPI ROM</b>	
			Engineer: <b>Tina Lee</b>	
Size Custom	Project Name <b>Rocky 40/50</b>			Rev 1.0
Date: <b>Thursday, March 27, 2008</b>		Sheet <b>25</b> of <b>94</b>		

5	4	3	2	1
D				
C				
B				
A				

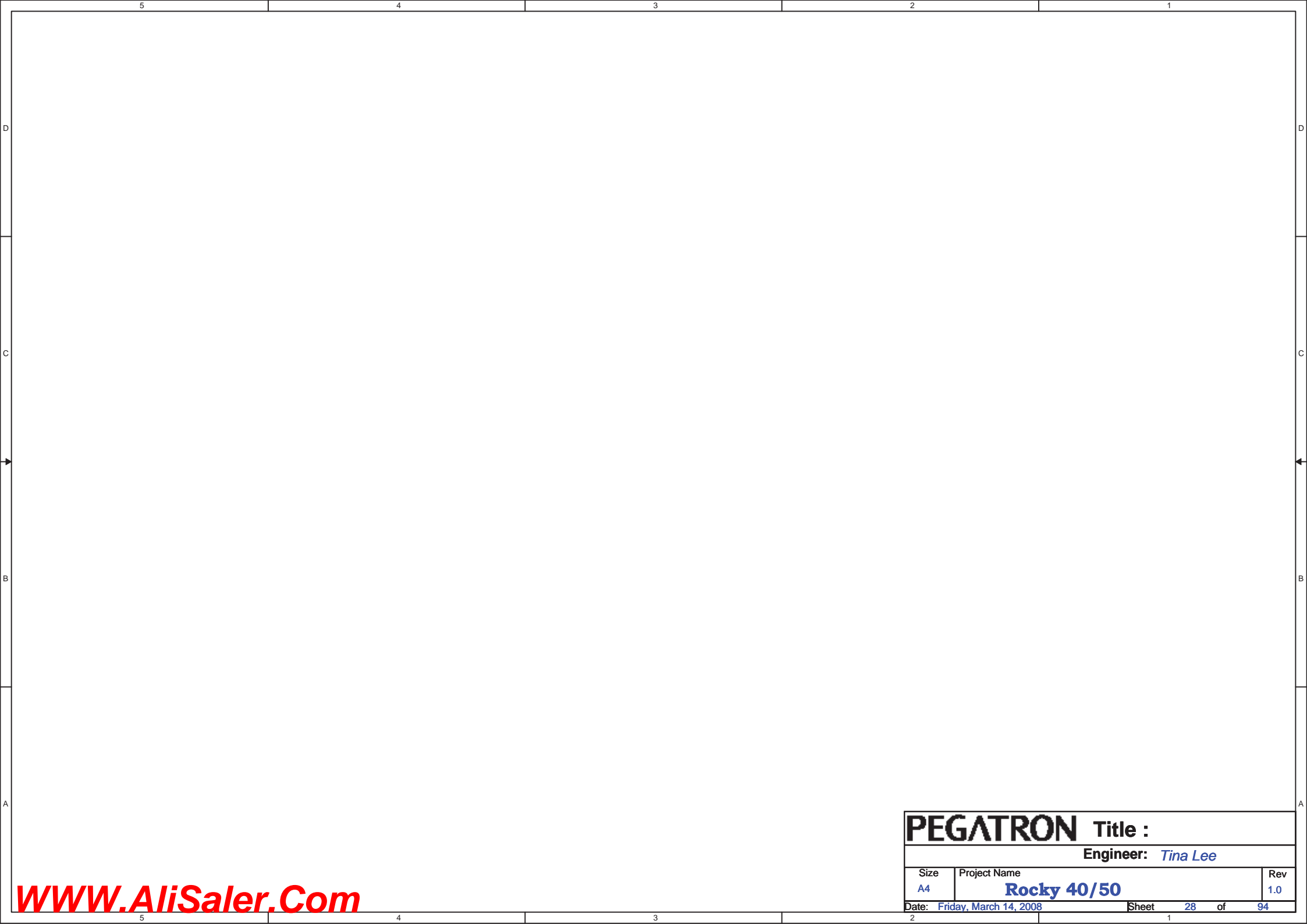
PEGATRON

Title :

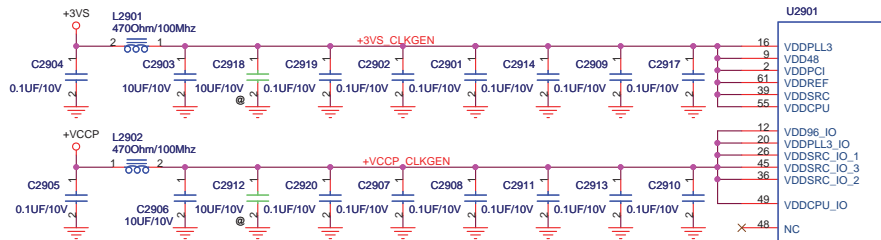
Engineer: Tina Lee

Size A4	Project Name Rocky 40/50	Rev 1.0
Date: Friday, March 14, 2008	Sheet 26 of 94	

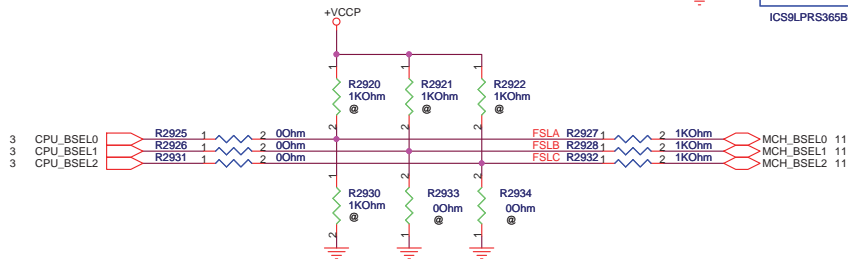
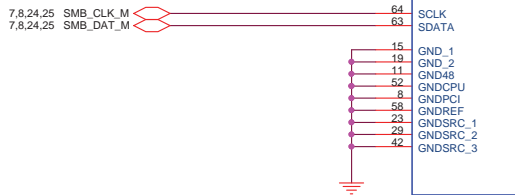
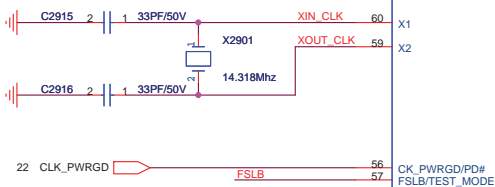
PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	27	of 94



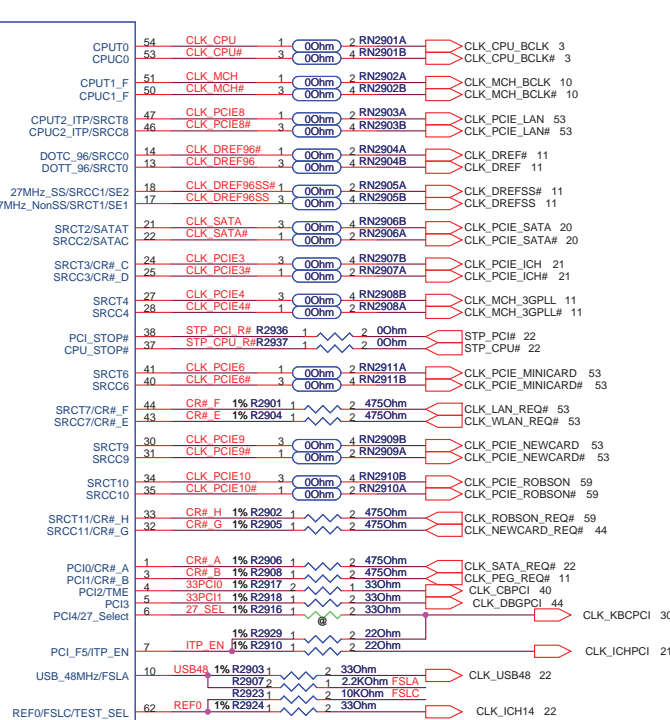
PEGATRON			Title :		
			Engineer: Tina Lee		
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	28	of 94



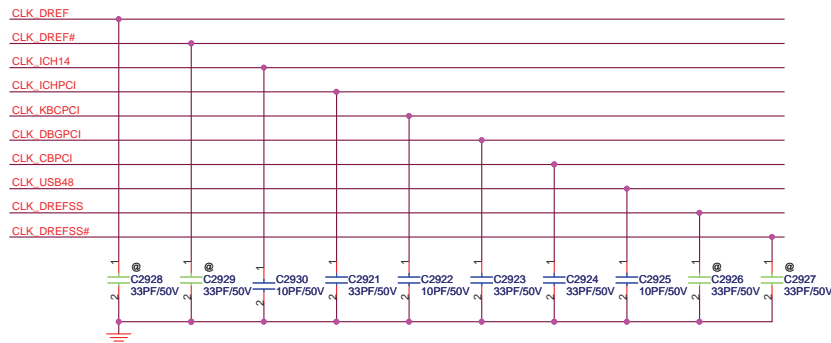
C2917, C2918, C2919 near CLK Gen.



BCLK	FSB	FSLC	FSLB	FSLA
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0



C2921, C2922, C2923, C2924, C2925, C2926, C2927, C2928, C2929, C2930 near CLK Gen.



CR#_A	0 = SRC 0	
	1 = SRC 2	SATA
CR#_B	0 = SRC 1	
	1 = SRC 4	MCH
CR#_C	0 = SRC 0	
	1 = SRC 2	
CR#_D	0 = SRC 1	
	1 = SRC 4	
CR#_E	SRC 6	WLAN
CR#_F	SRC 8	LAN
CR#_G	SRC 9	New Card
CR#_H	SRC 10	Robson

## Latched Input Select

0 = SRC 8      Decide pin  
1 = CPU\_ITP CLK      46, 47



27\_Select=0,      Decide pin  
pin#13/14=DOT96;      13/14, 17/18  
pin#17/18=LCD\_SST;

27\_Select=1,      Decide pin  
pin#13/14=SRC0;      13/14, 17/18  
pin#17/18=27MHz non-spread SE clock;



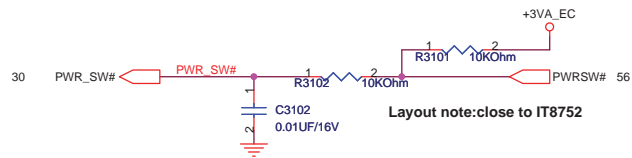
For GM/GL, need to PD for 96MHz output.  
For PM, need to PU for 27MHz output.





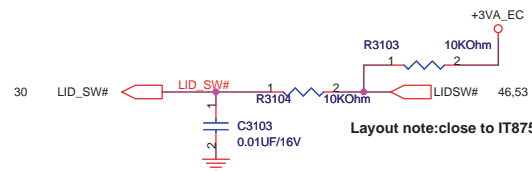
### For Switch

PWR  
SWITCH

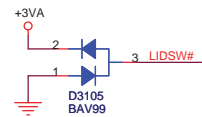


Layout note:close to IT8752

LID  
SWITCH



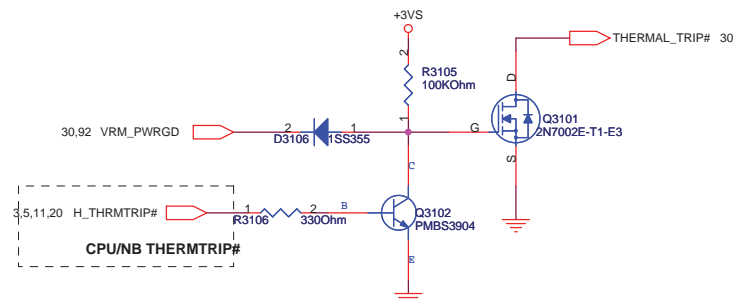
Layout note:close to IT8752



close to connector

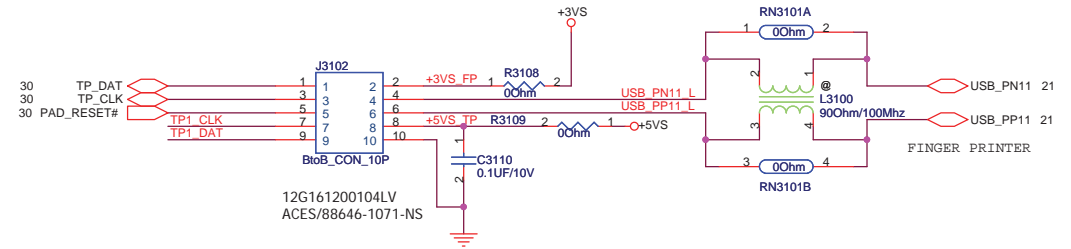
Note:  
LID\_SW# is easy to cause high voltage damage when  
plugging inverter board connector to M/B with AC present.  
Need to add bidirectional diode to protect this pin.

### For Thermal Control Method



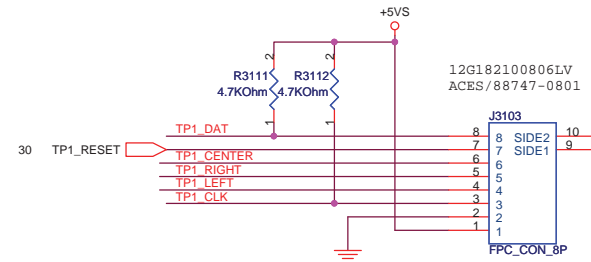
CPU/NB THERMTRIP#

## TOUCH PAD CONN

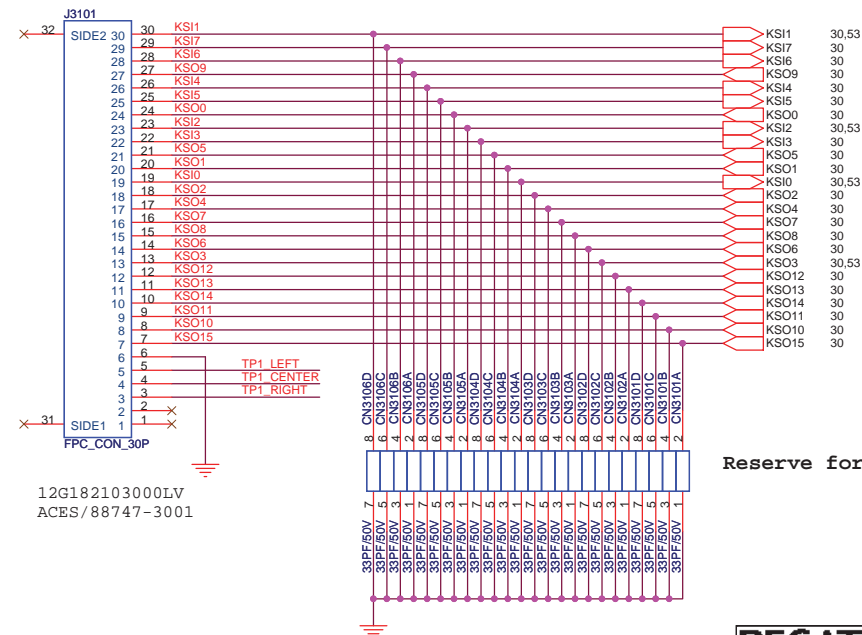


TP :Touch Pad  
TP1:Trach Point

## TRACK POINT CONN



## Keyboard Connector



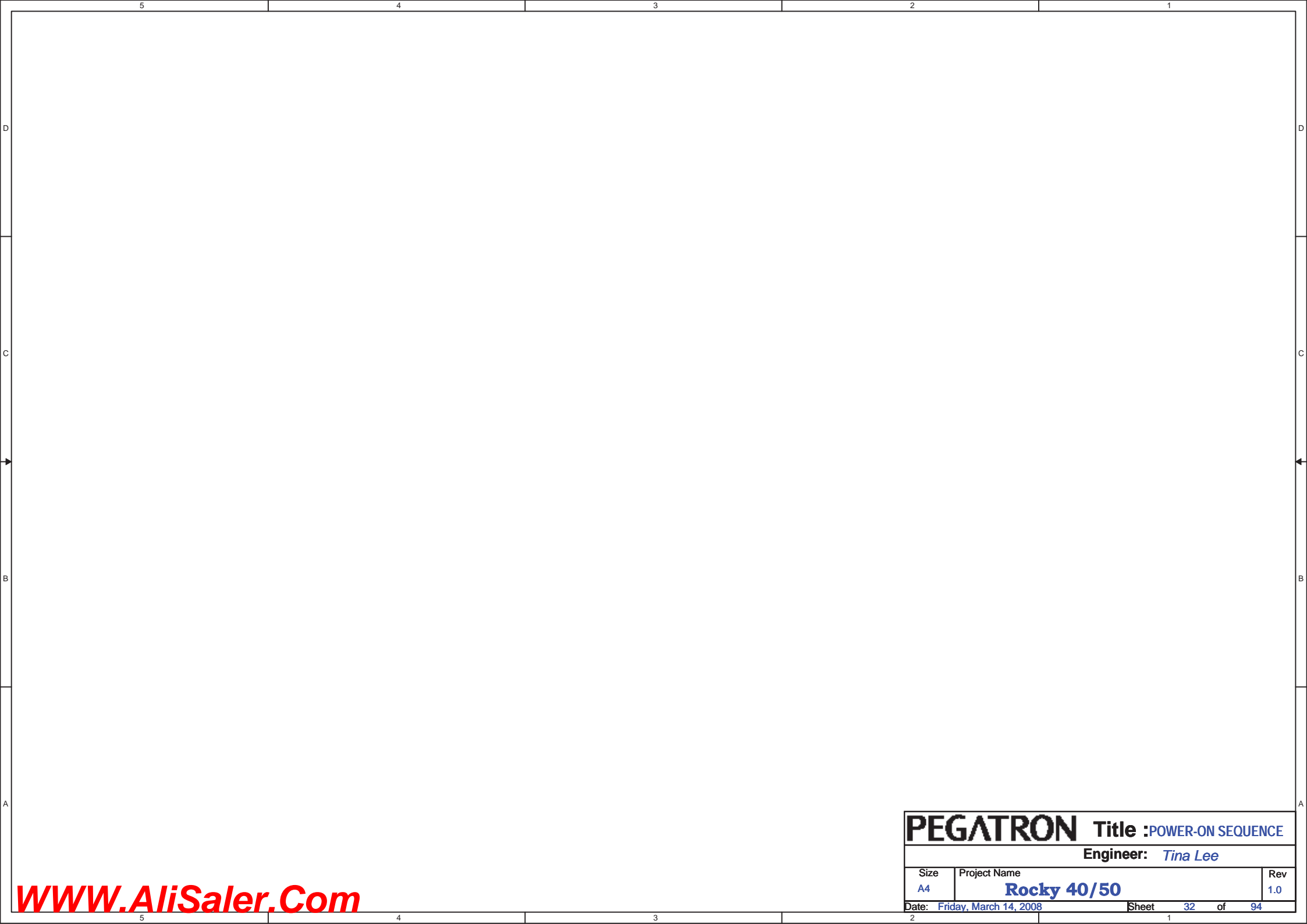
Reserve for WWAN

12G182103000LV  
ACES/88747-3001

**PEGATRON** Title : EC\_IT8752 (2/2)

Engineer: *Tina Lee*

Size	Project Name	Re
Custom	<b>Rocky 40/50</b>	1.0



PEGATRON		Title :POWER-ON SEQUENCE	
		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	32 of 94

5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : ****	
		Engineer: Tina Lee	
Size A4	Project Name Rocky 40/50		Rev 1.0
Date: Friday, March 14, 2008		Sheet	33 of 94

PEGATRON		Title : ****	
<Variant Name>		Engineer: Tina Lee	
Size	Project Name	Rev	
A4	Rocky 40/50	1.0	
Date: Friday, March 14, 2008		Sheet	34 of 94

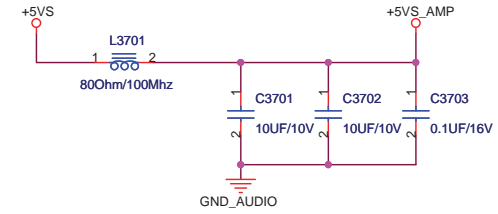
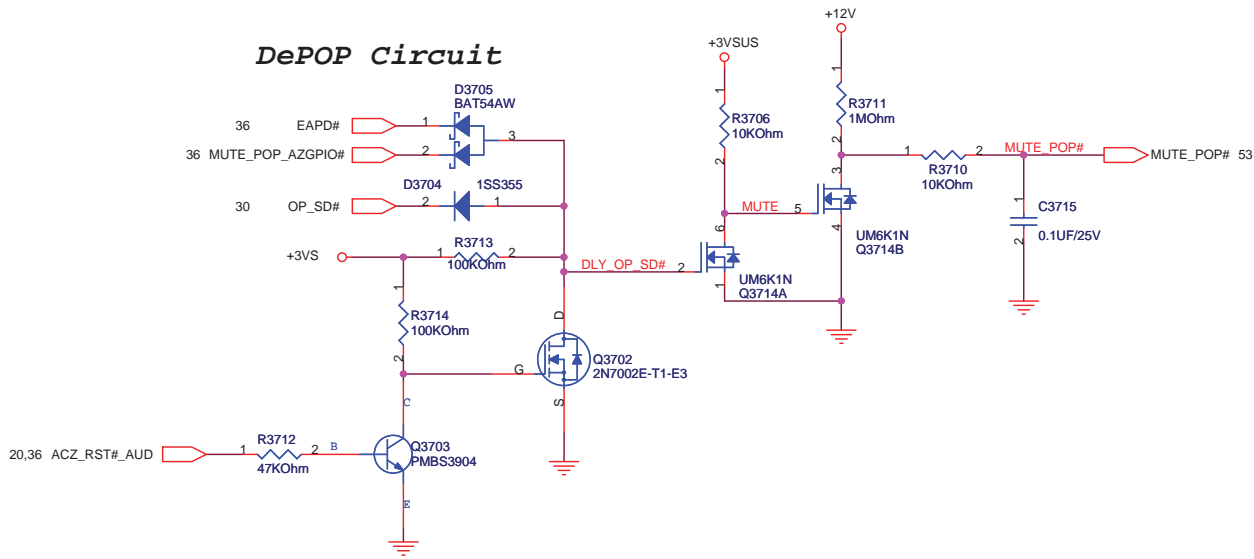
5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : MDC	
		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	35 of 94

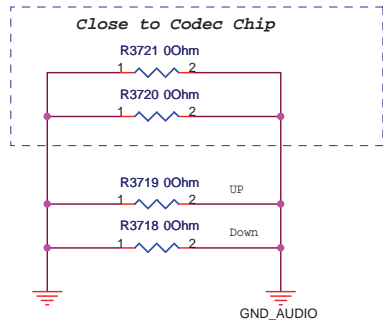




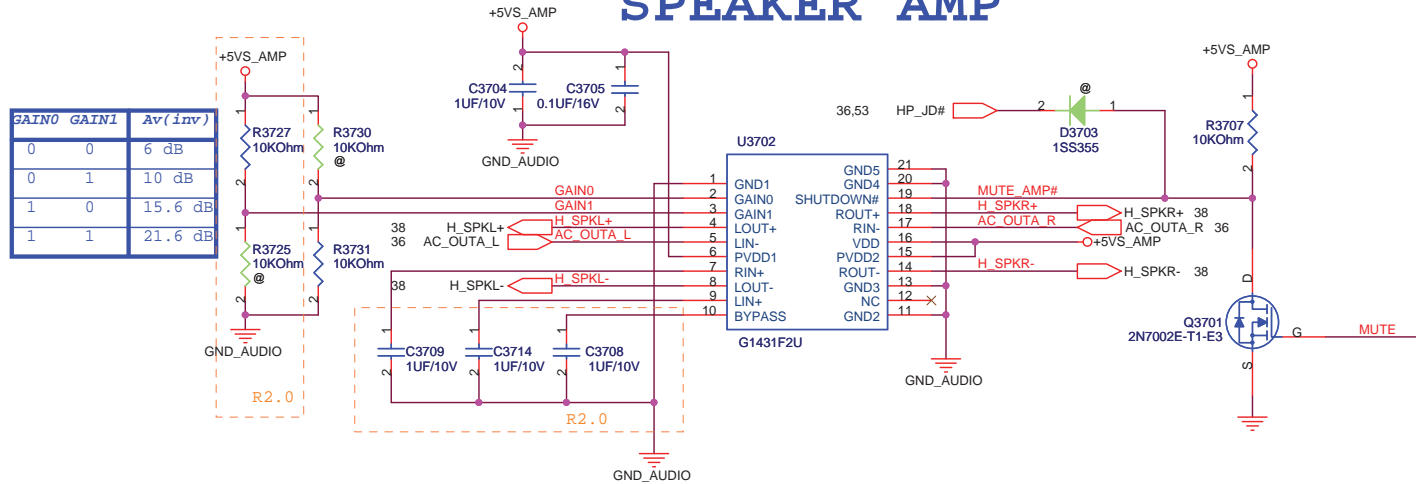
## DePOP Circuit



## JACK GND



## SPEAKER AMP

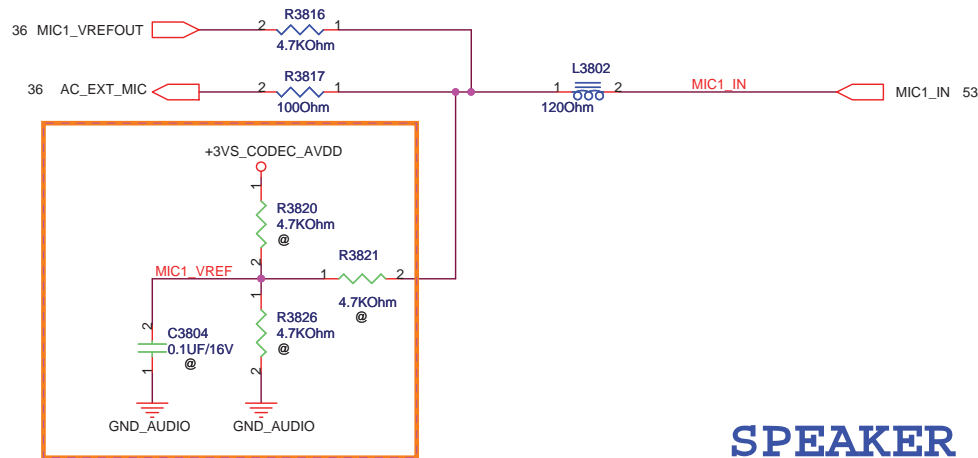


**PEGATRON** Title : **AUDIO AMP**

Engineer: **Tina Lee**

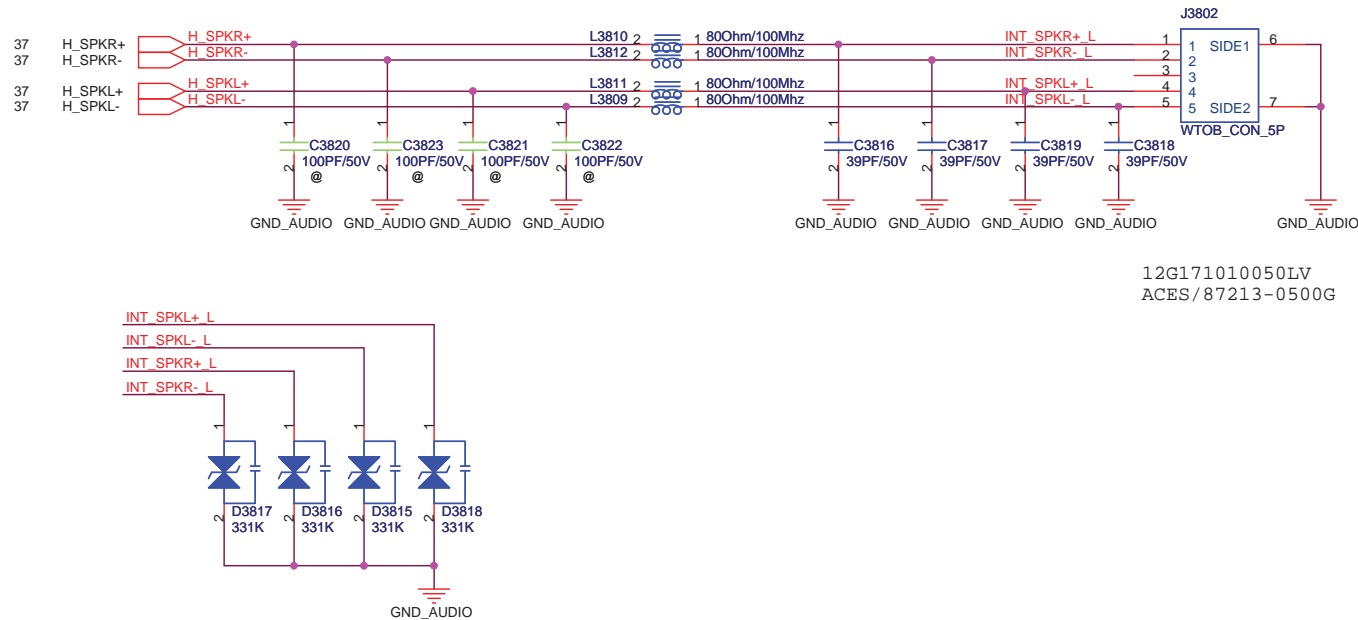
Size	Project Name	Rev
Custom	<b>Rocky 40/50</b>	1.0
Date: Thursday, March 27, 2008		Sheet 37 of 94

# EXT MICROPHONE



Reserved the external MIC bias(T filter).

# SPEAKER CONNECTOR

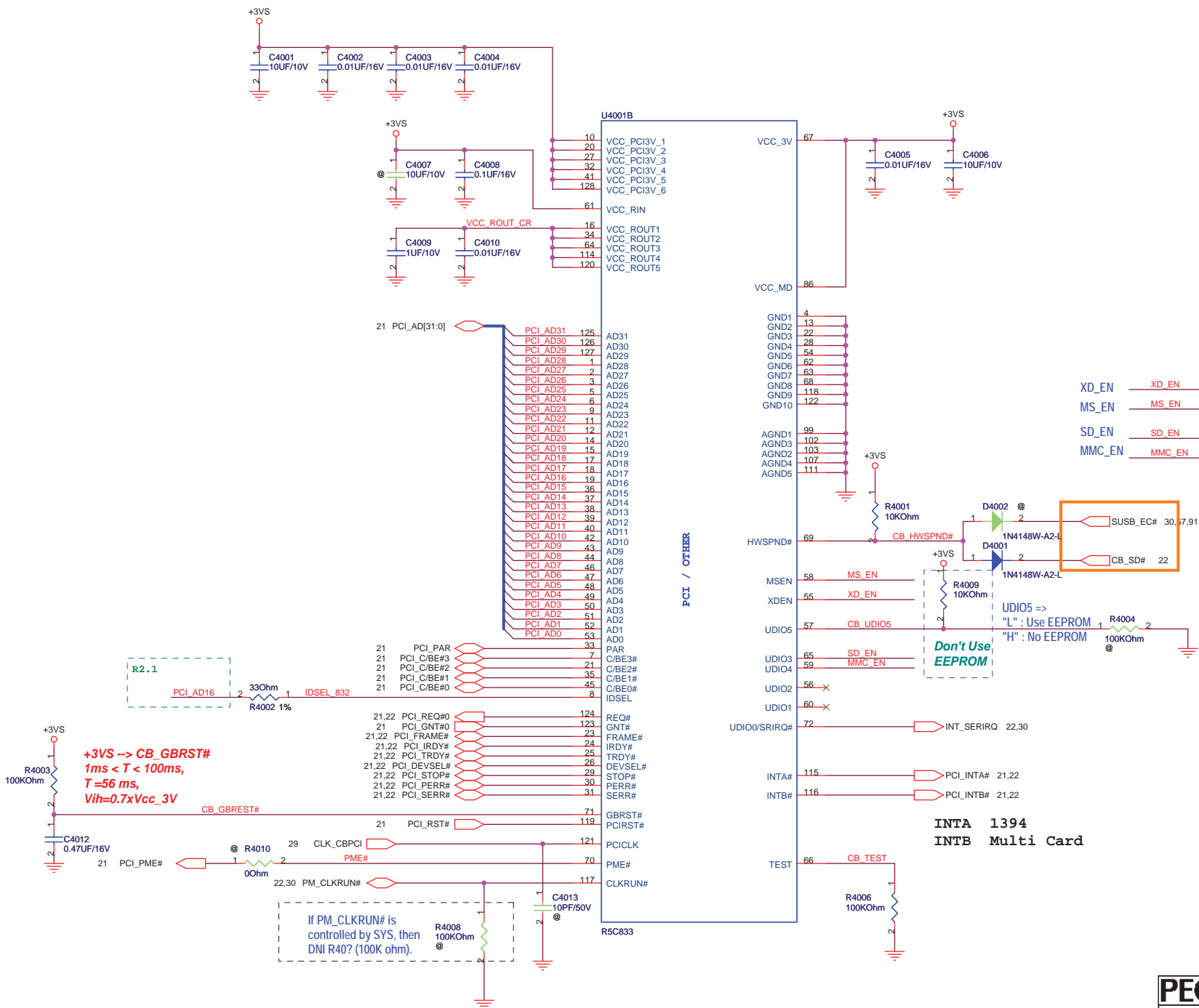


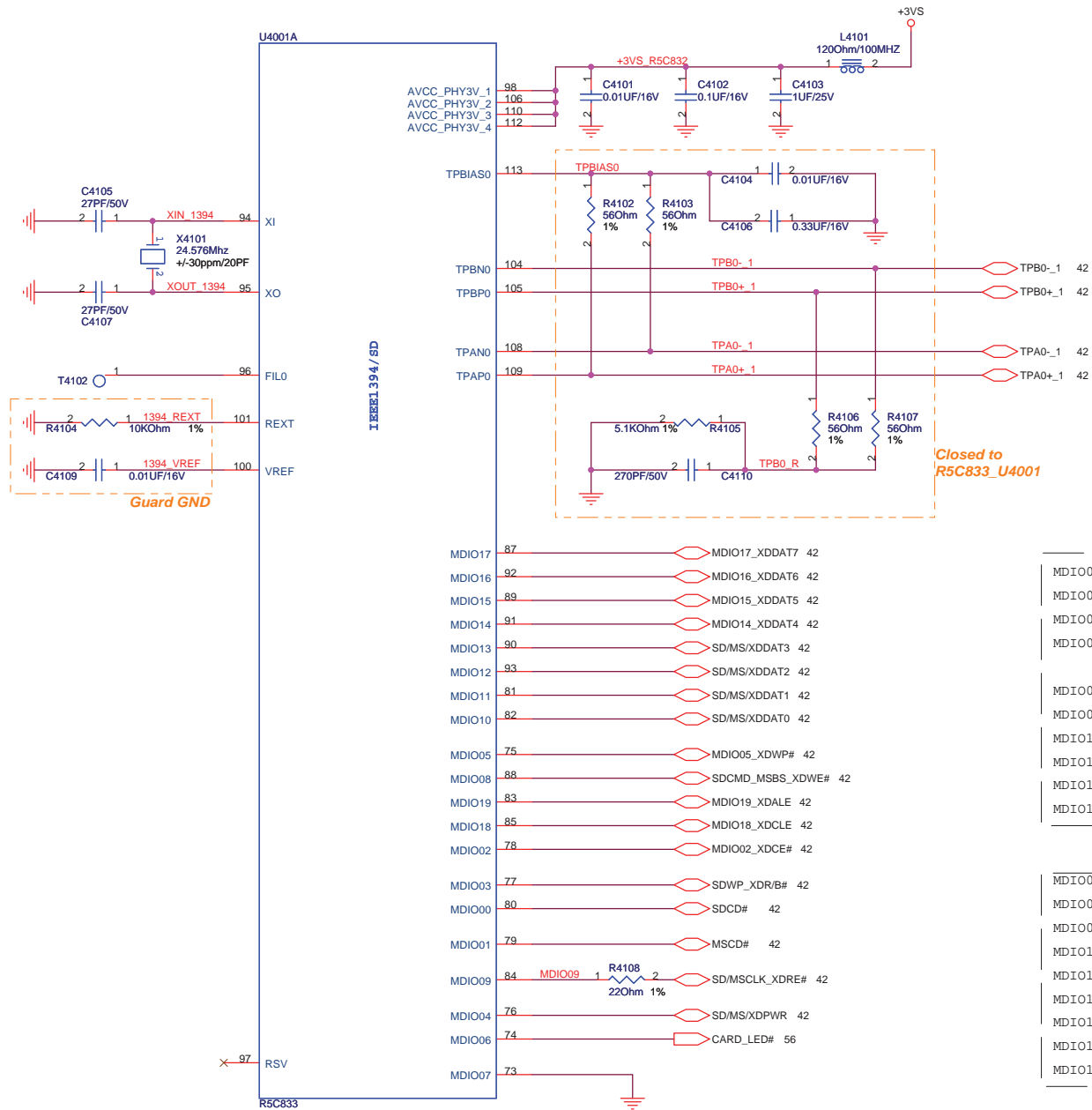
12G171010050LV  
ACES/87213-0500G

PEGATRON		Title : MIC&LINEIN	
Size		Engineer: Tina Lee	
Custom	Project Name	Rocky 40/50	
Date: Thursday, March 27, 2008		Sheet	38 of 94
		Rev	1.0

5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : FM2010 DSP	
		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008	Sheet	39	of 94





MDIO00--> SD Card Detect

MDIO01--> MS Card Detect

MDIO03--> SD Write Protect

MDIO04--> SD Card Power0 Control/  
MS Power Control

MDIO08--> SD Command/MS Bus State

MDIO09--> SD Clock/MS Clock

MDIO10--> SD Data 0/MS Data 0

MDIO11--> SD Data 1/MS Data 1

MDIO12--> SD Data 2/MS Data 2

MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#

MDIO05--> SD Power Control 1 / xDWP

MDIO06--> xD/MS/SD LED Control

MDIO14--> xD Data

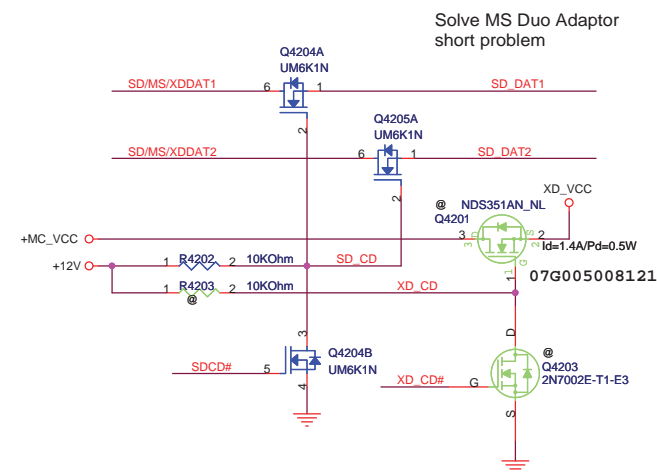
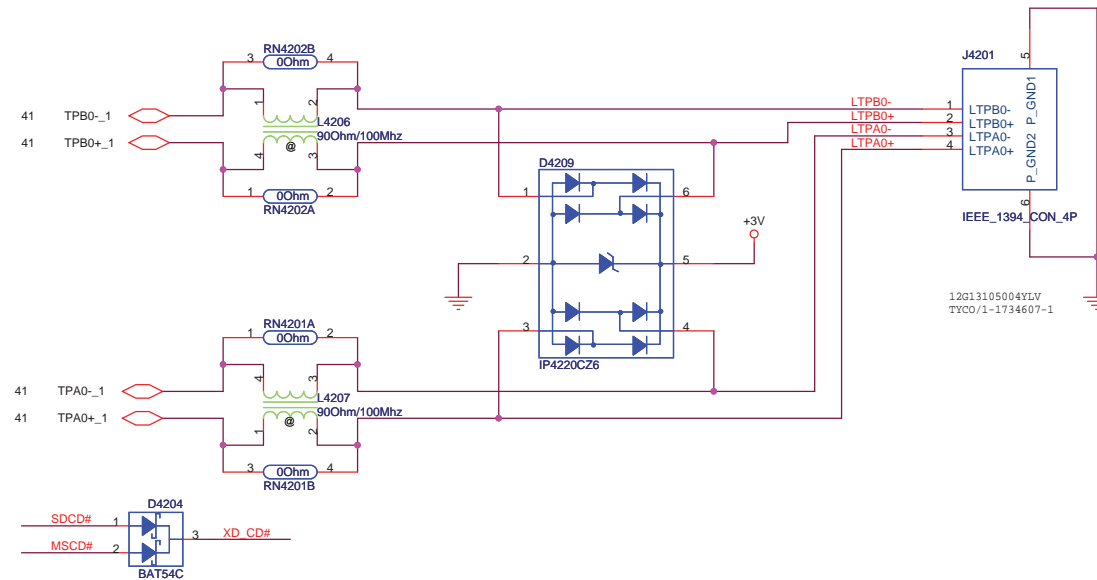
MDIO15--> xD Data

MDIO16--> xD Data

MDIO17--> xD Data

MDIO18--> xD CLE

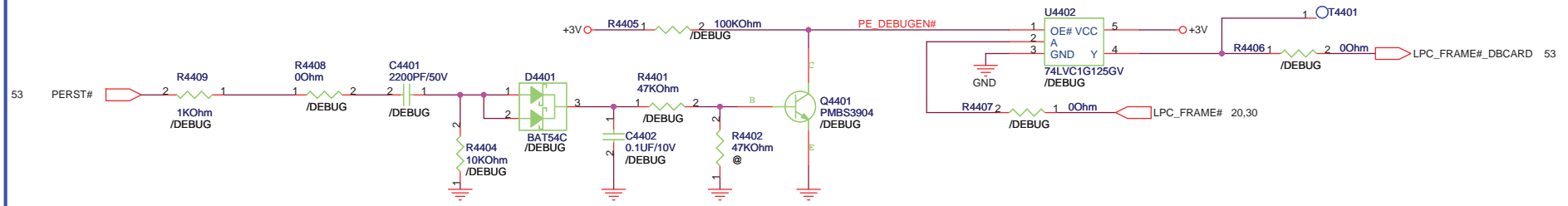
MDIO19--> xD ALE



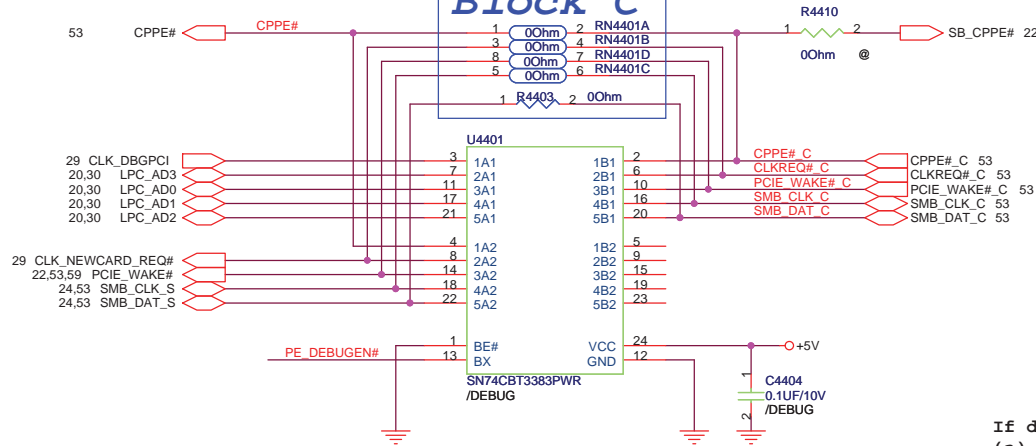
5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : NEW CARD	
		Engineer: Tina Lee	
Size A4	Project Name Rocky 40/50		Rev 1.0
Date: Friday, March 14, 2008		Sheet	43 of 94

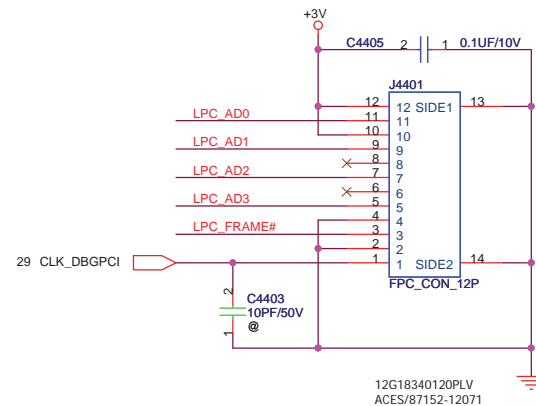
## Block A



## Block C

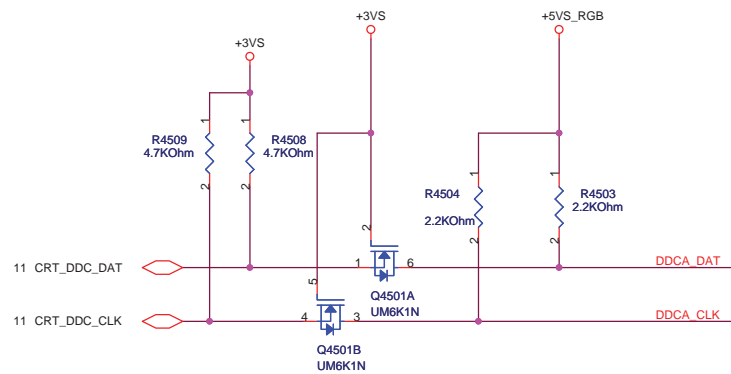
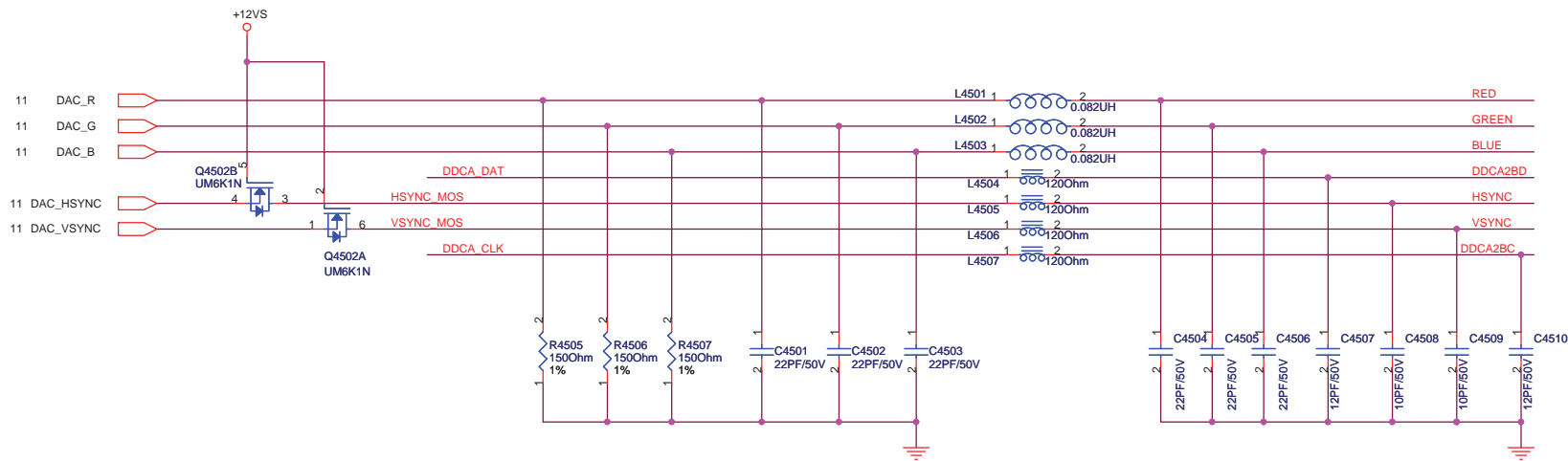


If don't support NewCard Debug Card,Pls do  
(a) DNI all components of block A  
(b) Mount Block C (RN5401,R6975)

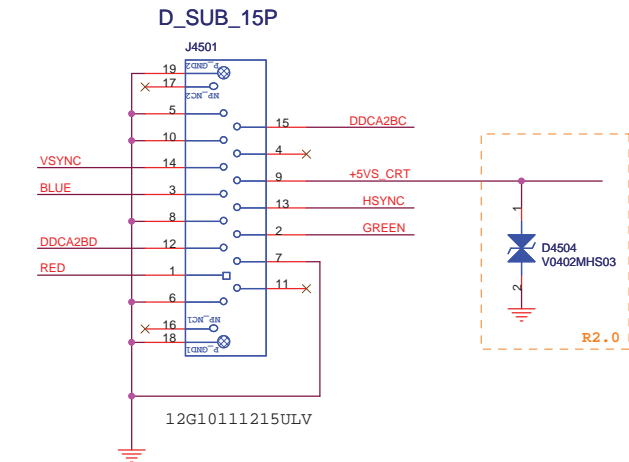
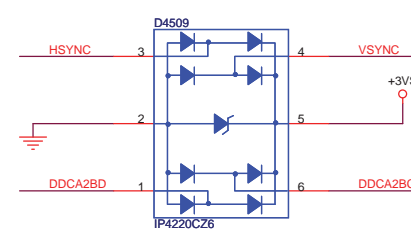
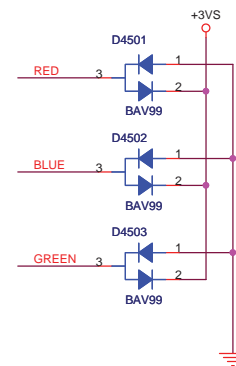


PEGATRON		Title : DEBUG	
Size		Engineer: Tina Lee	
Custom	Project Name	Rocky 40/50	
Date: Thursday, March 27, 2008	Sheet	44	of 94
		Rev	1.0

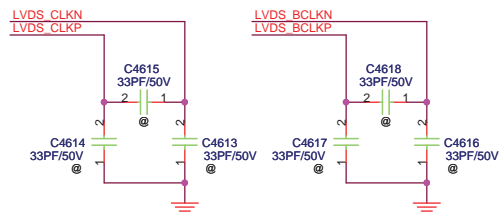
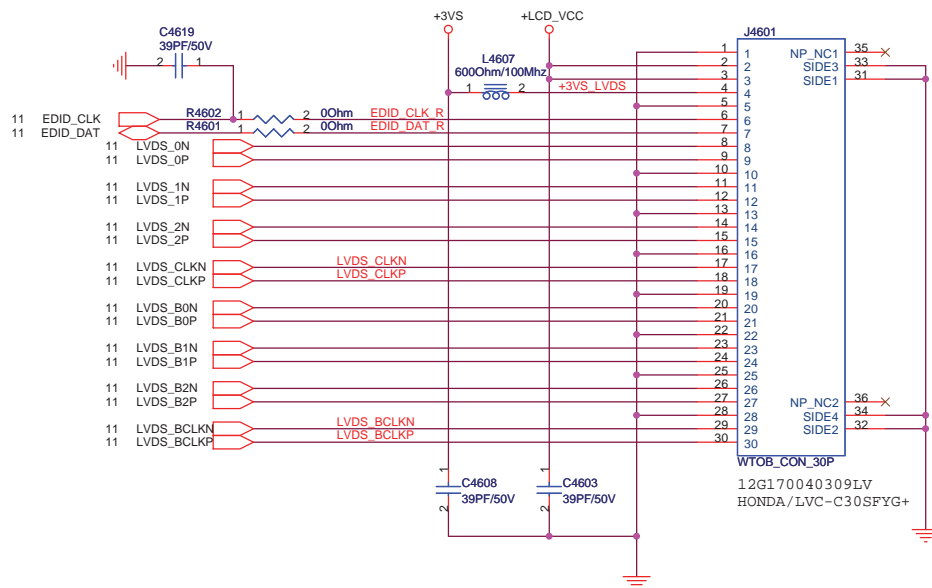




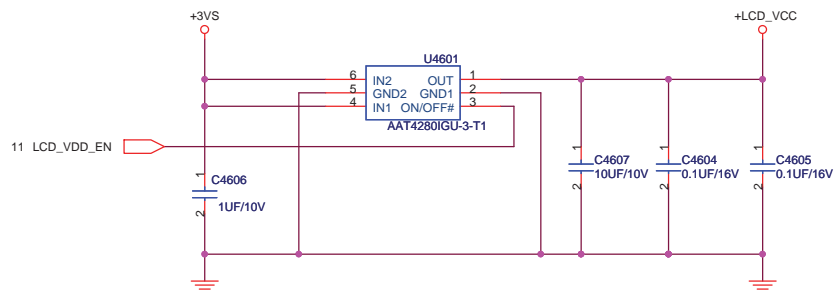
PLACE ESD Diodes near VGA port



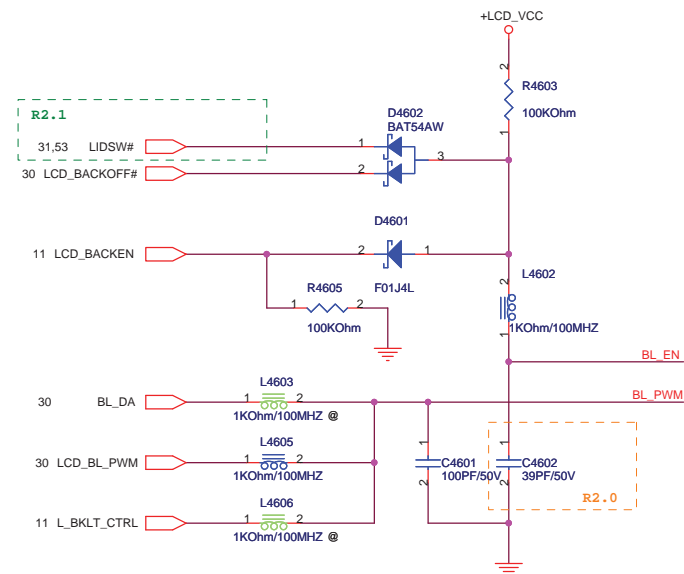
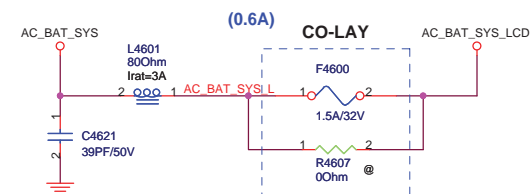
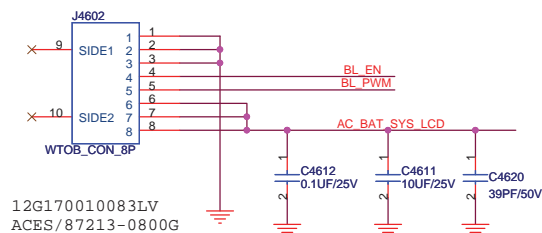
## LVDS CNT



## Power Switch for LCD Power



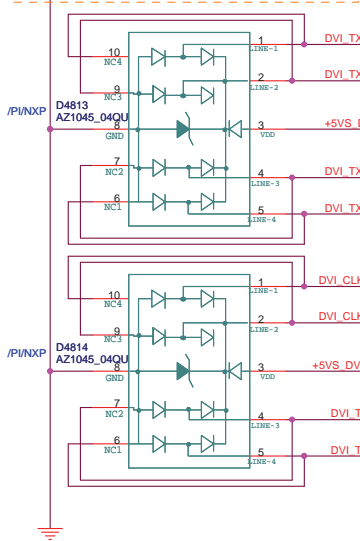
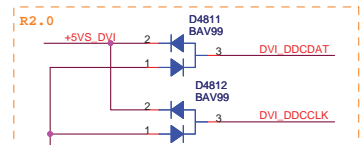
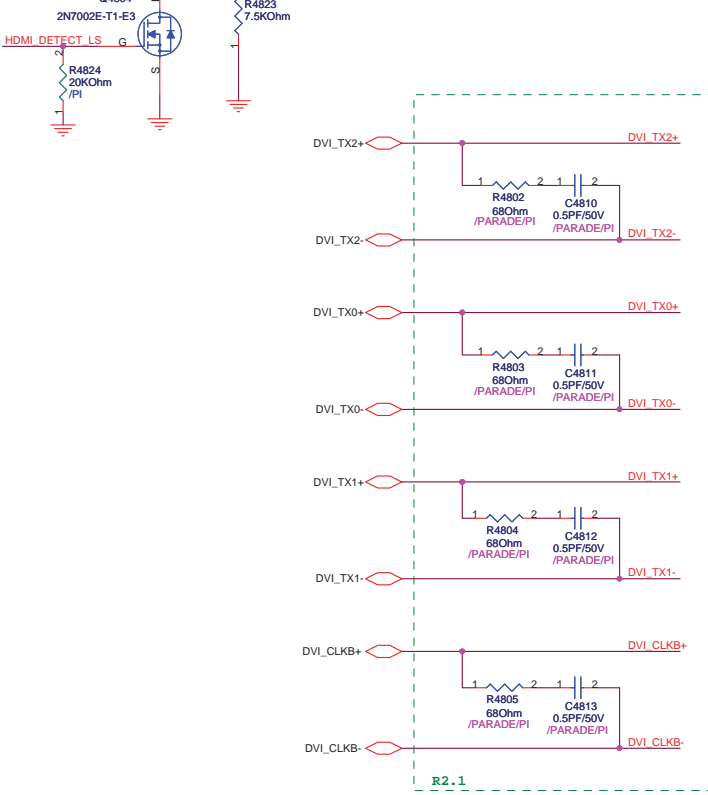
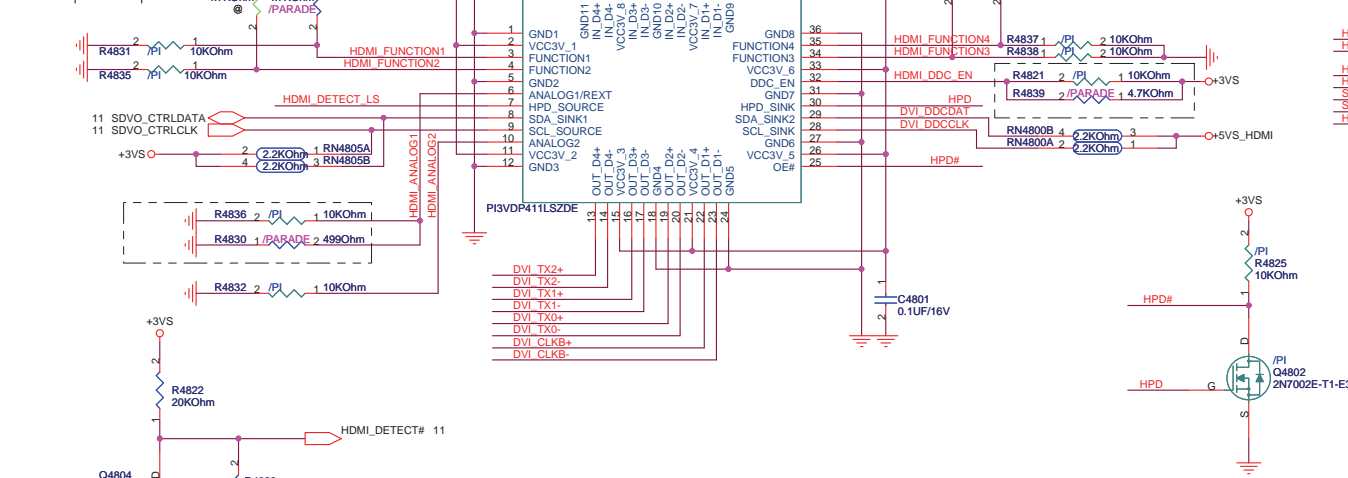
## INVERTOR CNT

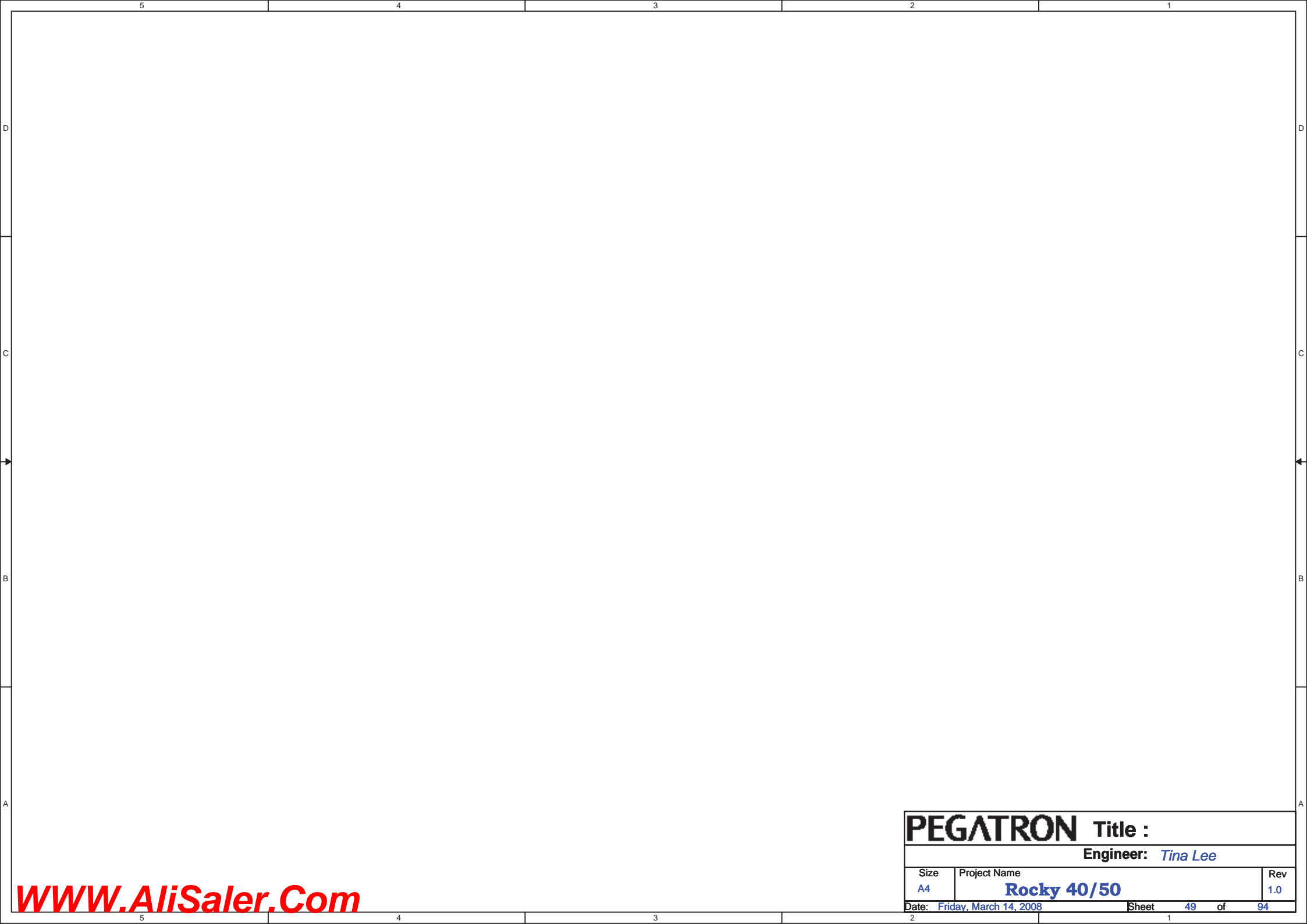


5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : TV_OUT CON	
		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet	47 of 94

	R4833	R4831
PI	@	10K
PARADE	4.7K	@
NXP	10K	@





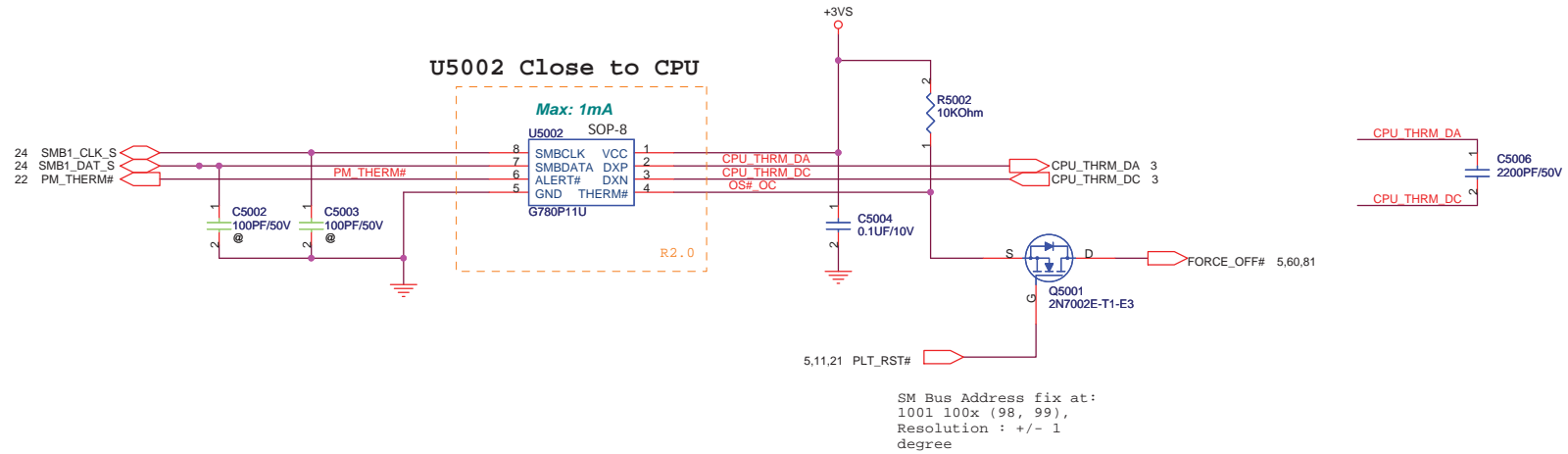
PEGATRON

Title :

Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 49 of 94	

# Thermal Sensor



## U5003 Close to SB and DIMM (Remove after DV Stage)

3.0V-5.5V  
Max: 1mA

U5003 mSOP-8

8 SMBCLK VCC  
7 SMBDATA DXP  
6 ALERT# DXN  
5 GND THERM#  
G781-1P8F

SMB1\_CLK\_S  
SMB1\_DAT\_S  
T5018

1 NB\_THERM\_DXP  
2 NB\_THERM\_DCN  
3 OS#\_OC

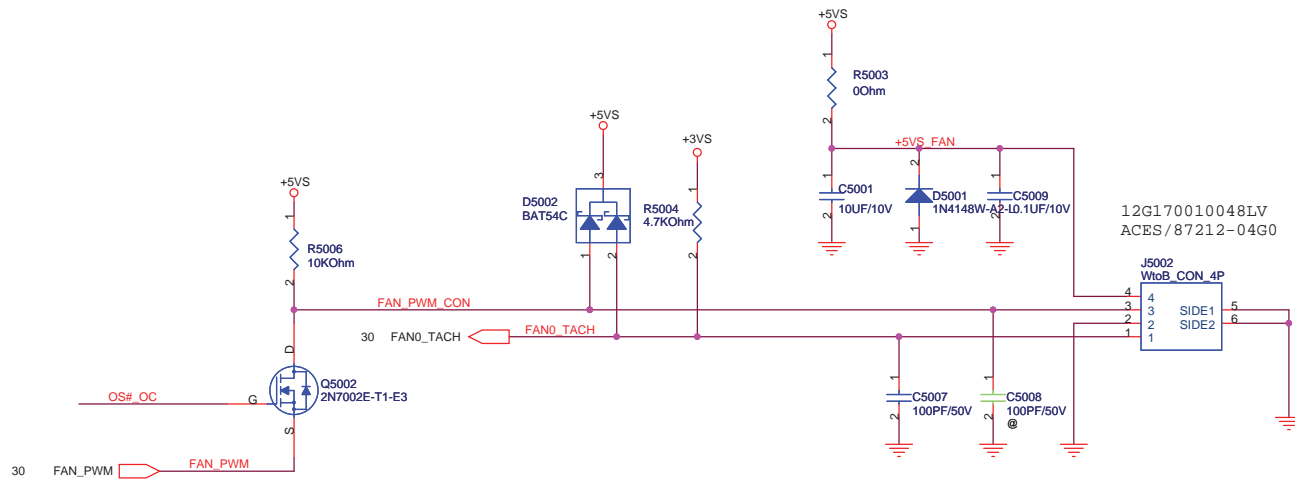
C5098 0.1UF/10V

SM Bus Address fix at:  
1001 101x (9A, 9B),  
Resolution : +/- 1  
degree

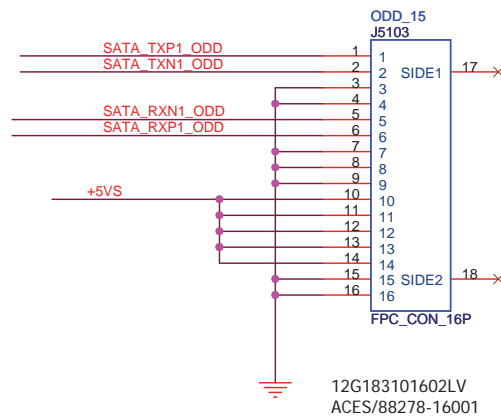
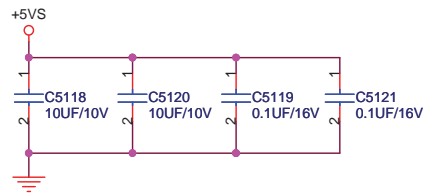
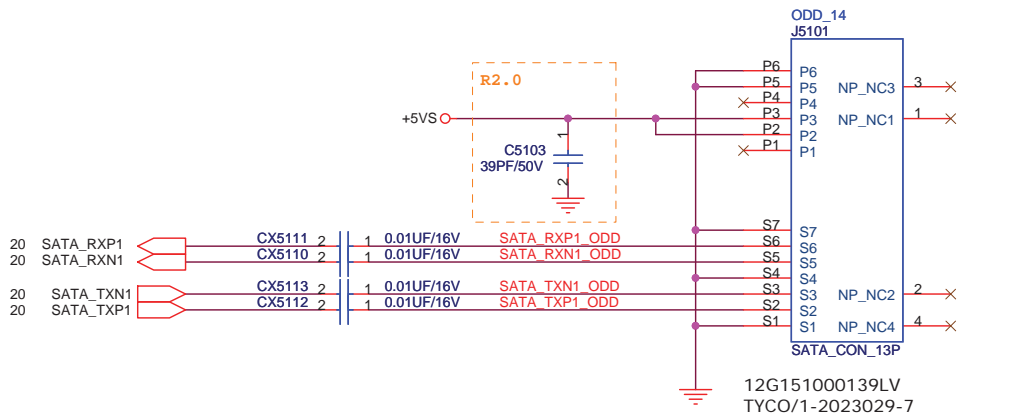
## Q5003 Close NB

C5097 2200PF/50V

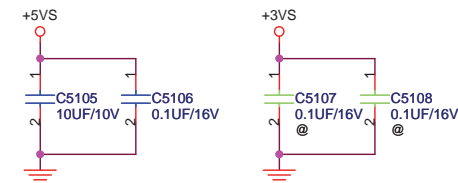
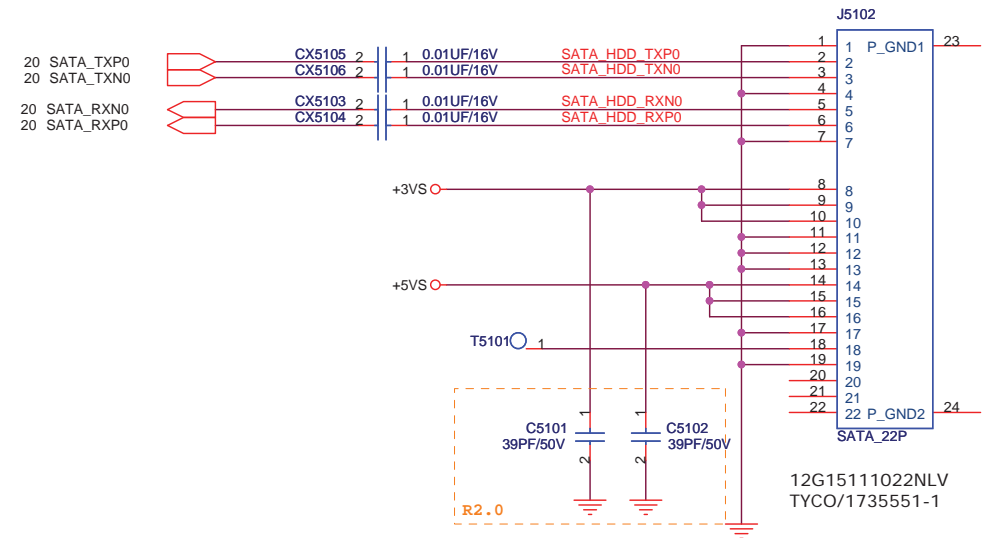
Q5003 PMBS3904

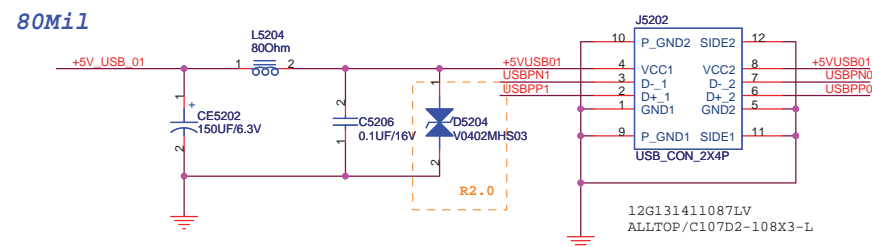
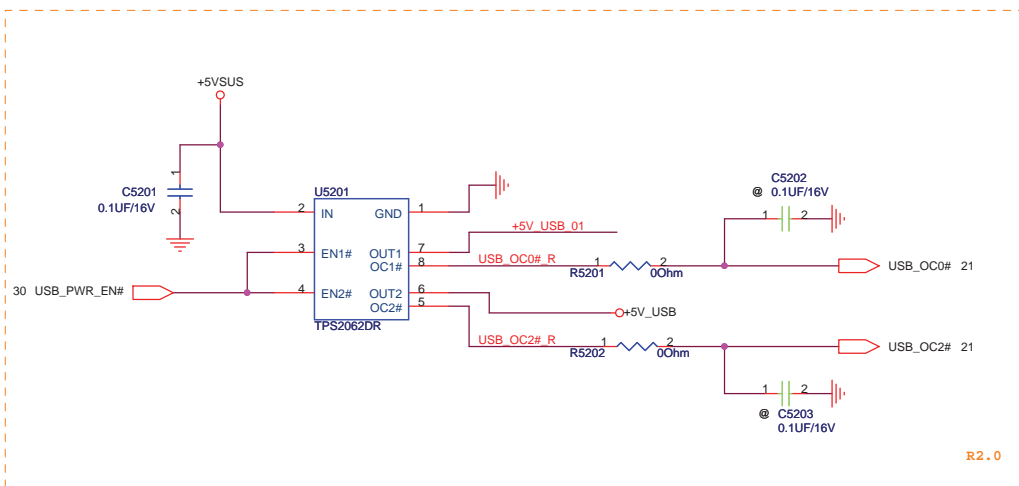
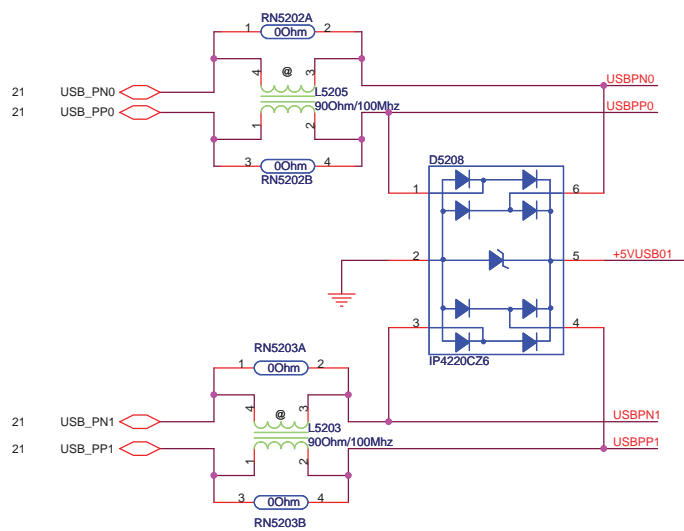


## ODD CON



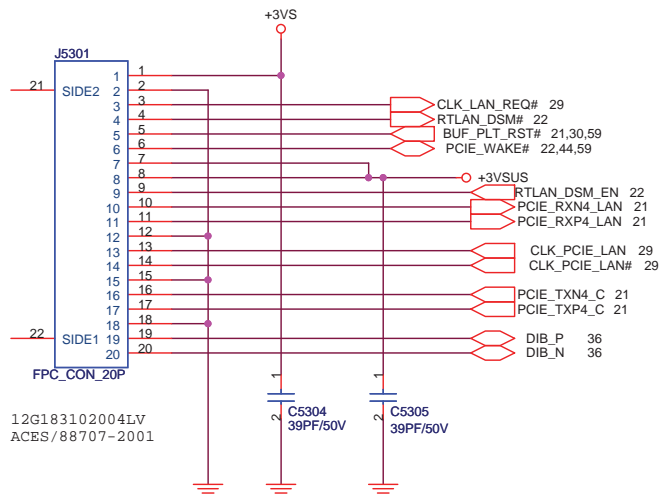
## SATA HDD CON



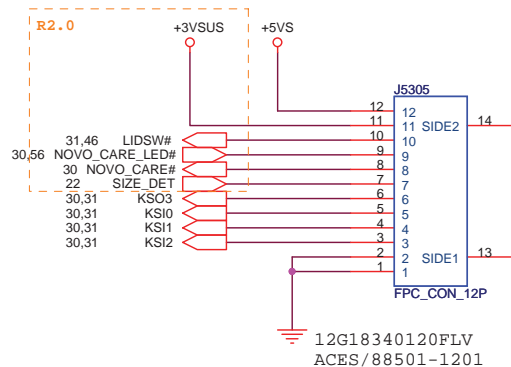




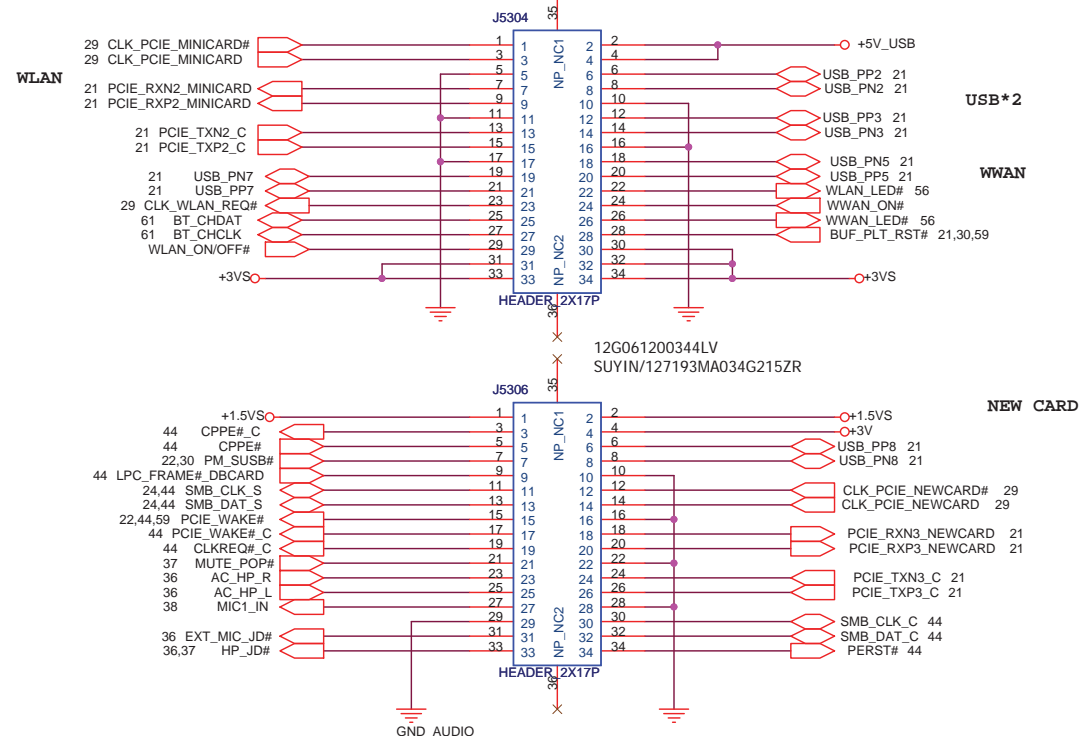
## IO BOARD



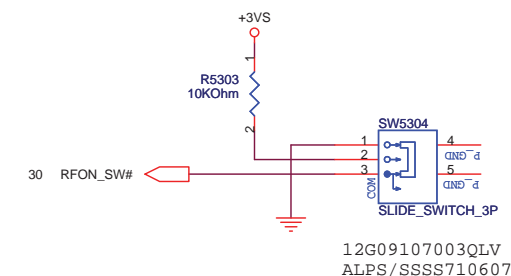
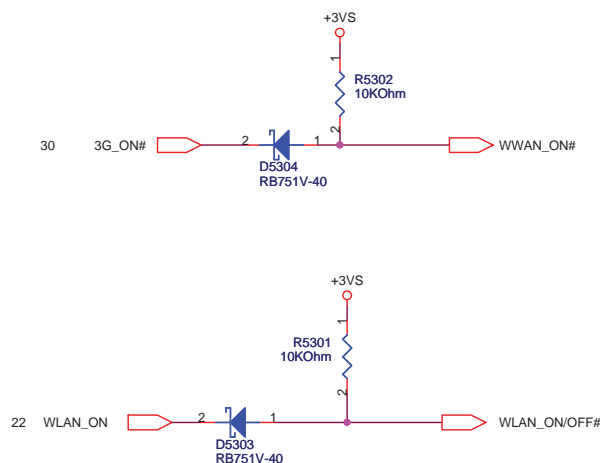
## For Media Control Board



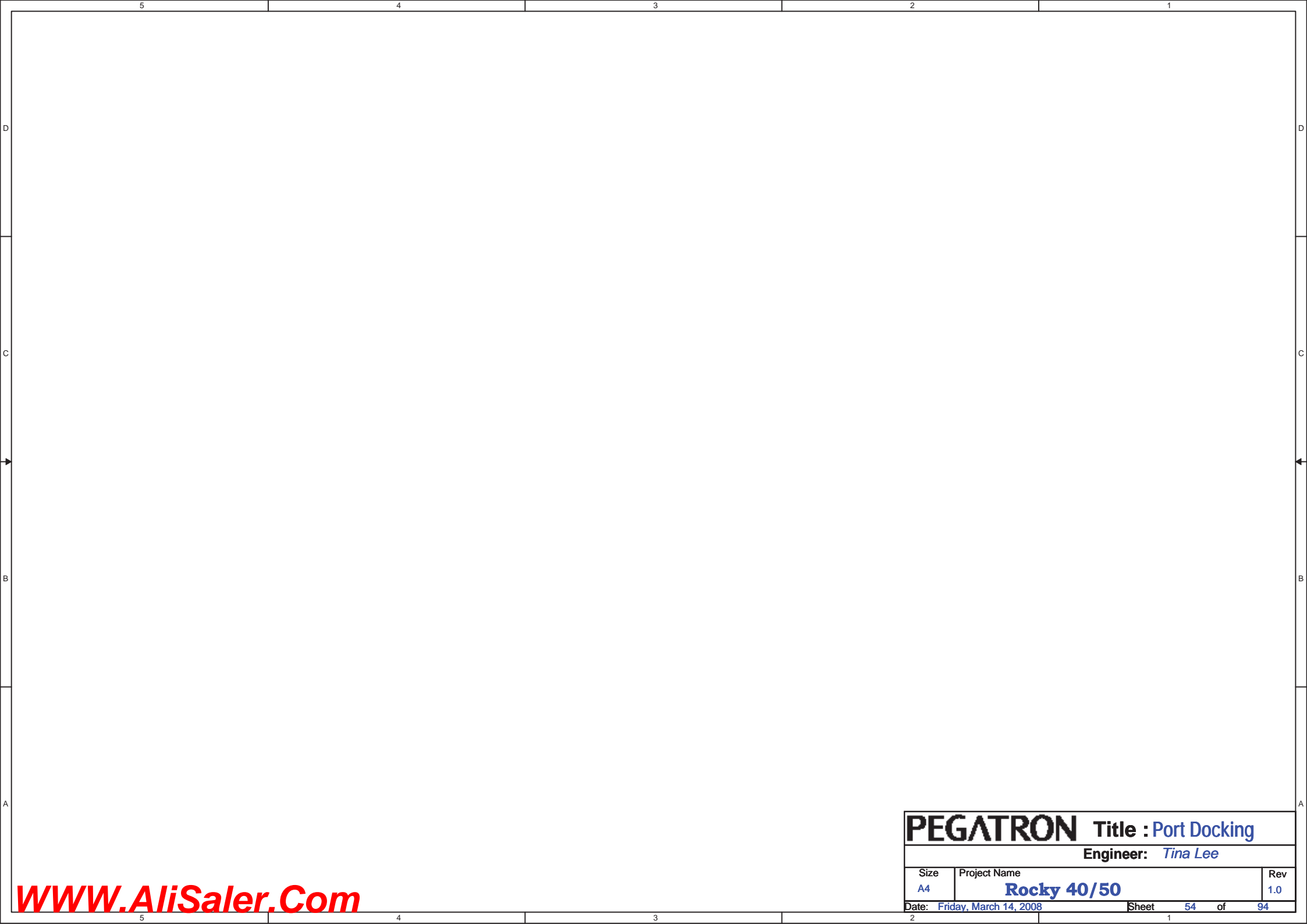
## SMALL BOARD



## Wireless Switch



<b>PEGATRON</b>		Title : <b>IO BOARD</b>	
		Engineer: <b>Tina Lee</b>	
Size Custom	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: <b>Thursday, March 27, 2008</b>		Sheet <b>53</b> of <b>94</b>	



PEGATRON

Title : Port Docking

Engineer: Tina Lee

Size A4	Project Name Rocky 40/50	Rev 1.0
Date: Friday, March 14, 2008	Sheet 54 of 94	

A

B

C

D

E

1

1

2

2

3

3

4

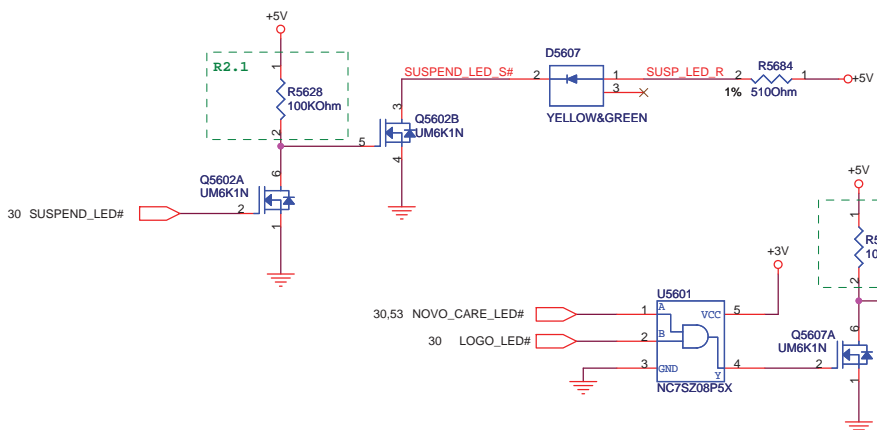
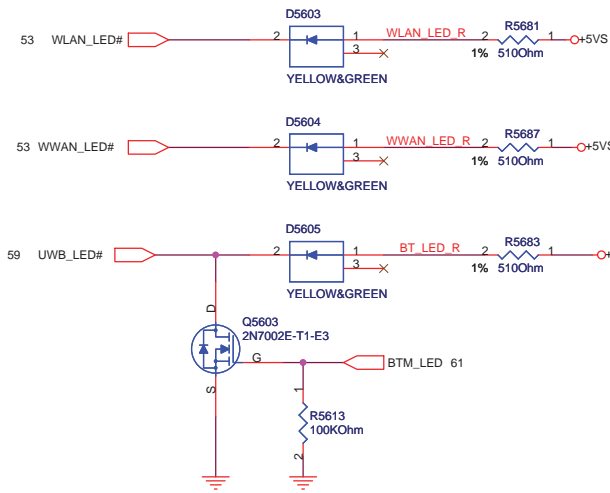
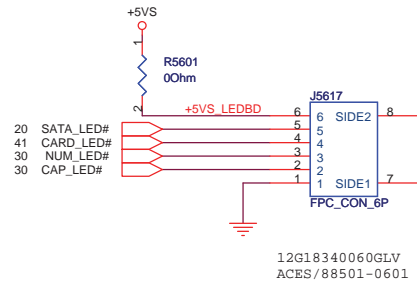
4

5

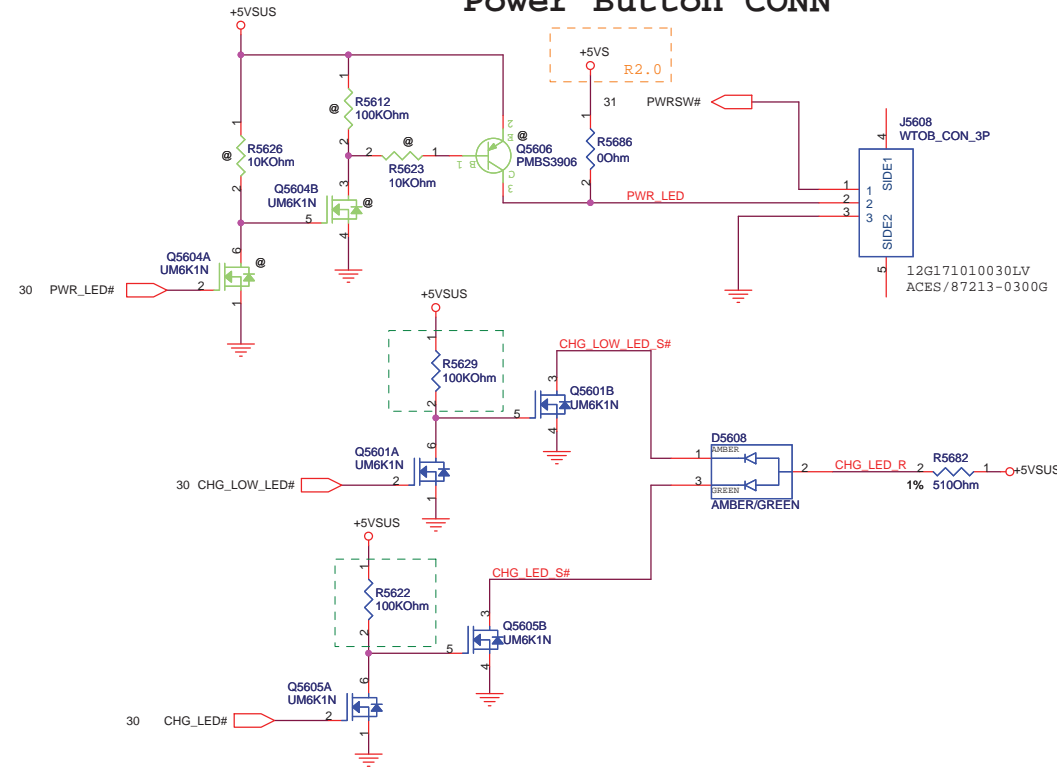
5

<b>PEGATRON</b>		<b>Title :</b> Super I/O & FIR	
<b>Engineer:</b> Tina Lee			
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008		Sheet 55 of 94	

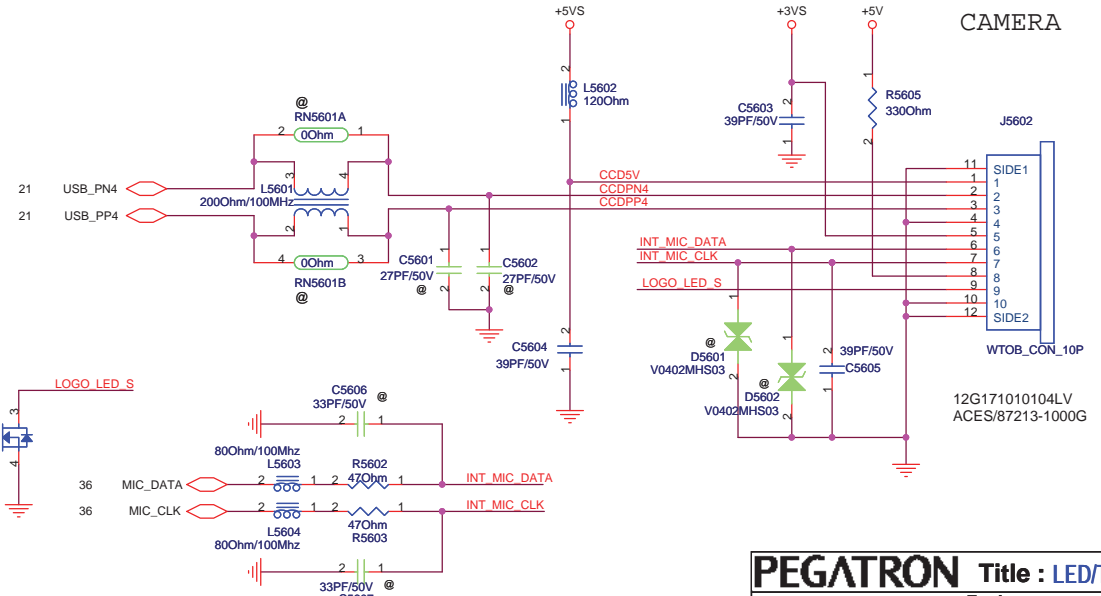
## LED CONN



## Power Button CONN

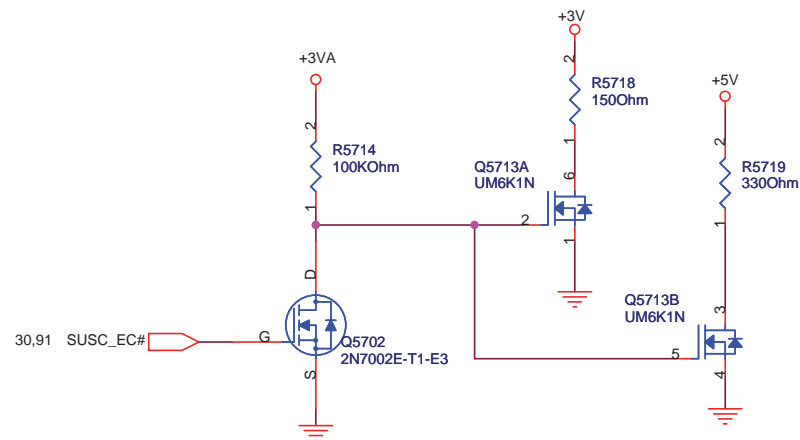
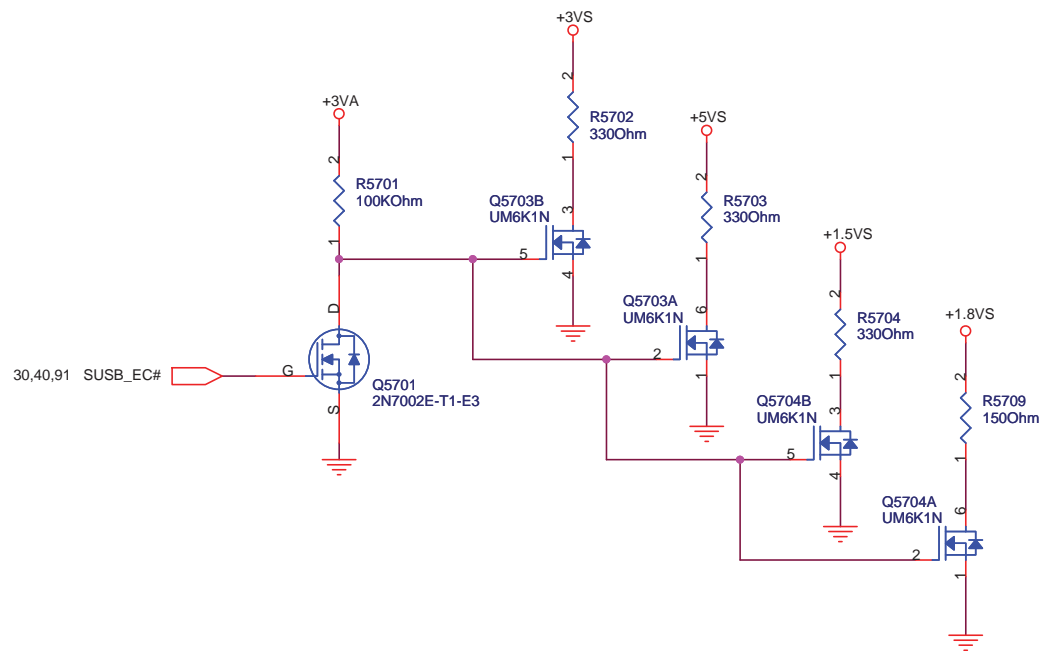


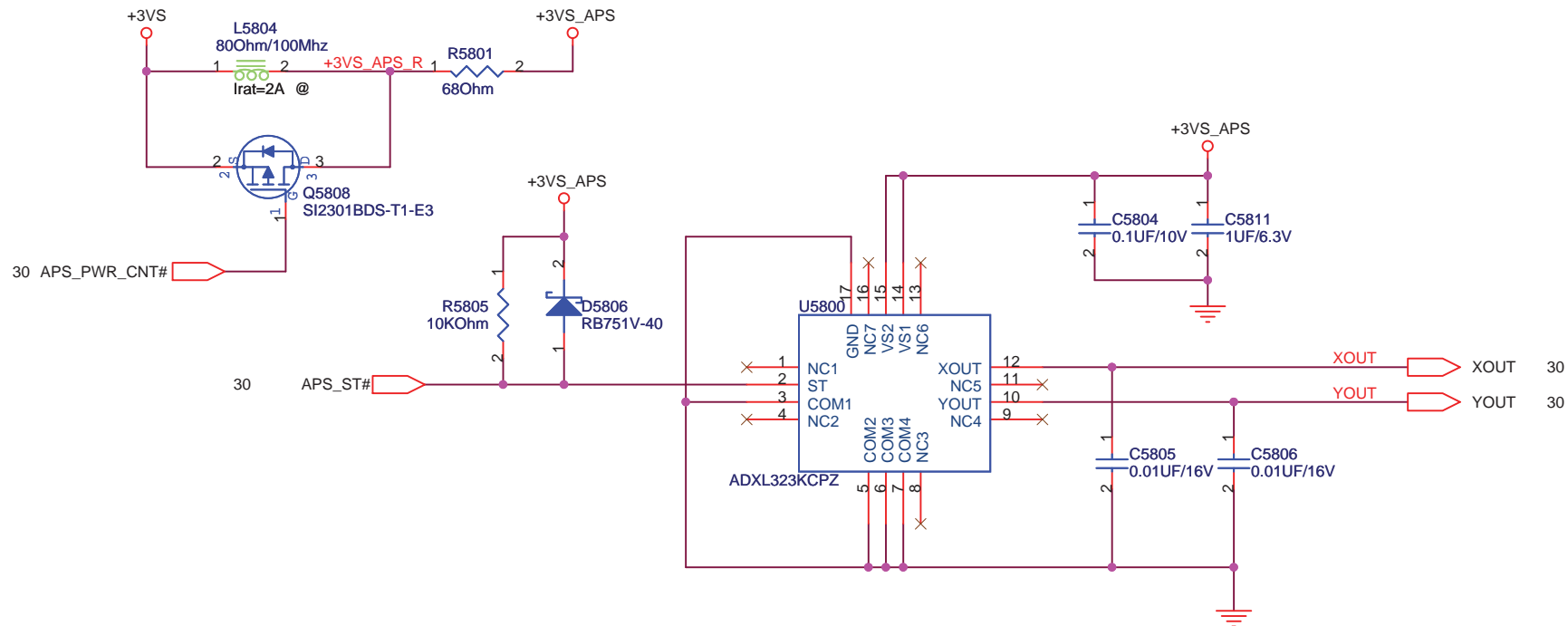
## CAMERA

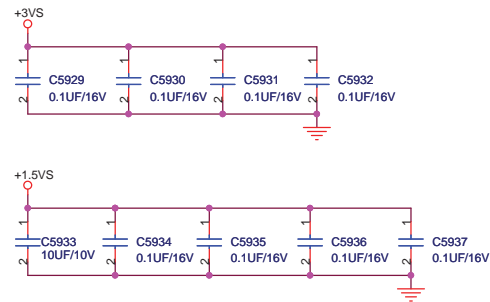
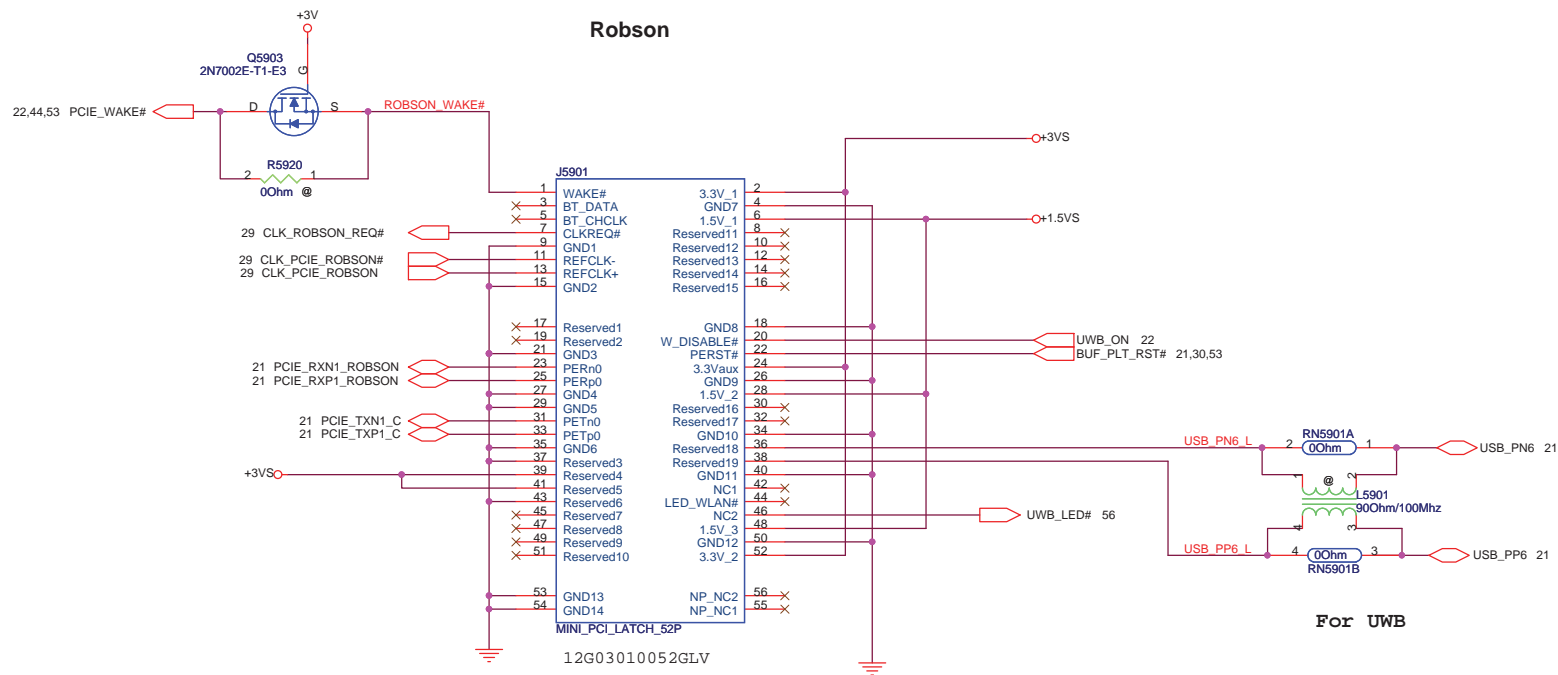


**PEGATRON** Title : LED/TP/SW  
Engineer: Tina Lee

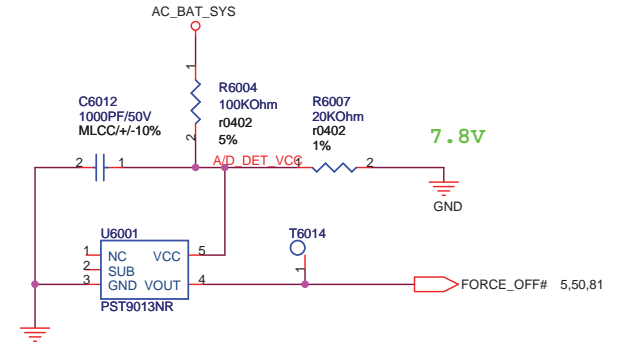
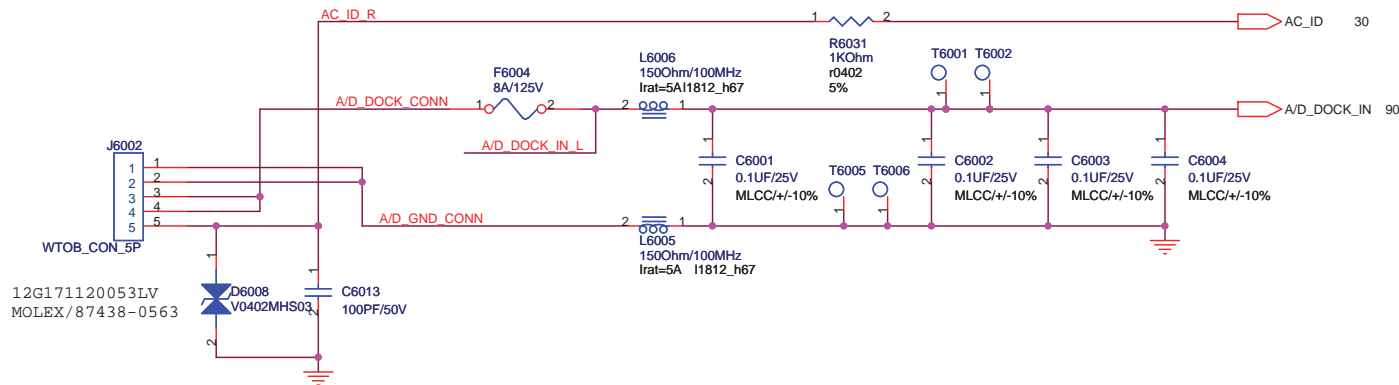
Size	Project Name	Rev
Custom	Rocky 40/50	1.0
Date: Thursday, March 27, 2008	Sheet 56 of 94	





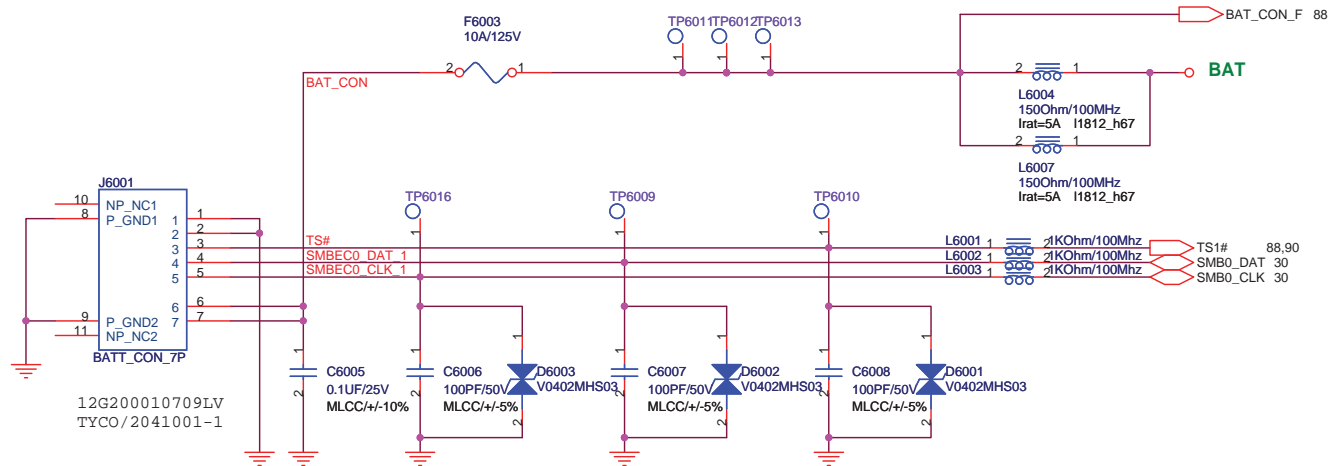


## DC IN CONN



Without Battery & Pull out Adapter

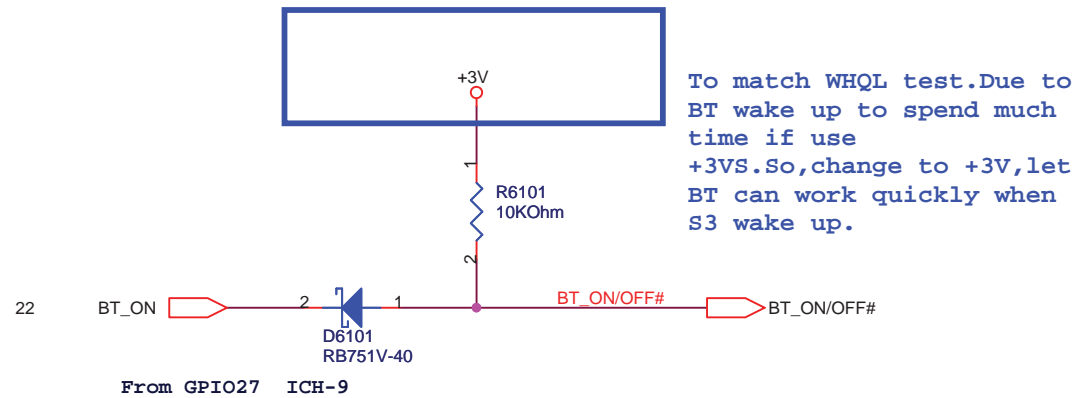
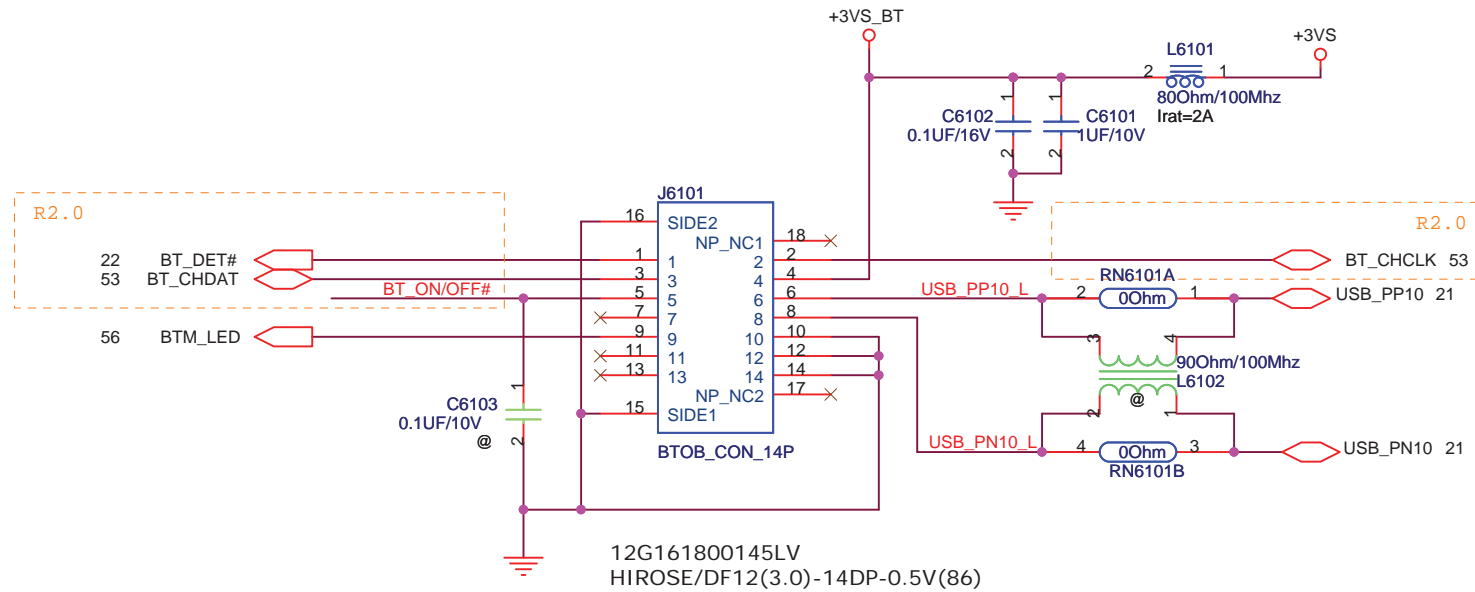
## Battery CONN



PEGATRON		Title : DC Jack & Battery CONN	
Size		Engineer: Morris Tseng	
Custom	Project Name	Rocky40/50	
Date: Thursday, March 27, 2008	Sheet	60	of 94
		Rev	1.0



# Blue Tooth



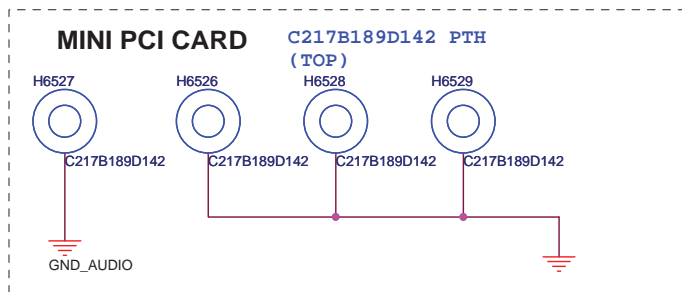
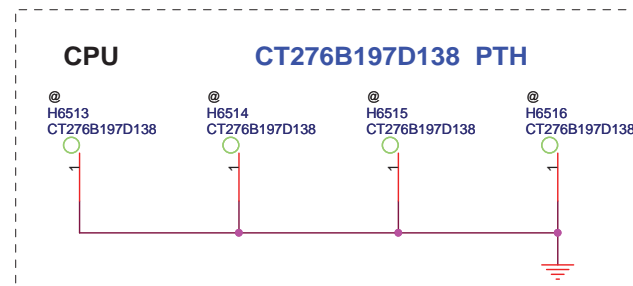
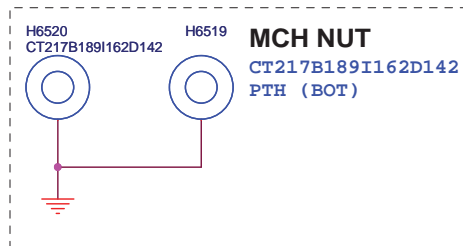
5	4	3	2	1
D				
C				
B				
A				

<b>PEGATRON</b>		Title : <b>TPM</b>	
Engineer: <i>Tina Lee</i>			
Size <b>A4</b>	Project Name <b>Rocky 40/50</b>		Rev <b>1.0</b>
Date: <b>Friday, March 14, 2008</b>		Sheet <b>62</b> of <b>94</b>	

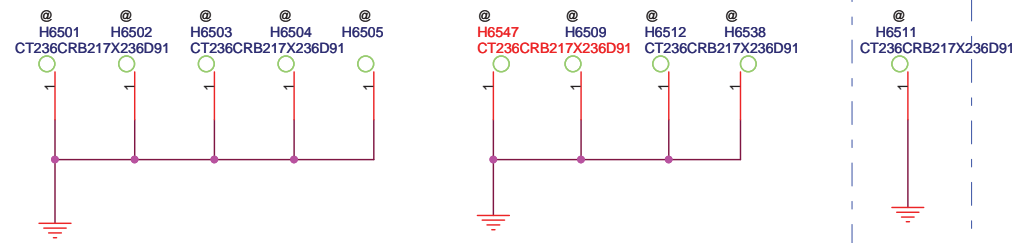


5	4	3	2	1
D				
C				
B				
A				

PEGATRON Title :		
Engineer: Tina Lee		
Size A4	Project Name Rocky 40/50	Rev 1.0
Date: Friday, March 14, 2008	Sheet 64	of 94



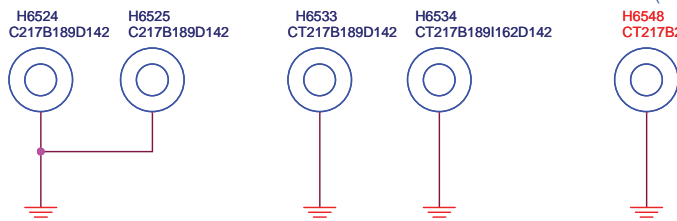
**MLB BOT - TOP SCREW HOLE**  
CT236CRB217X236D91 PTH



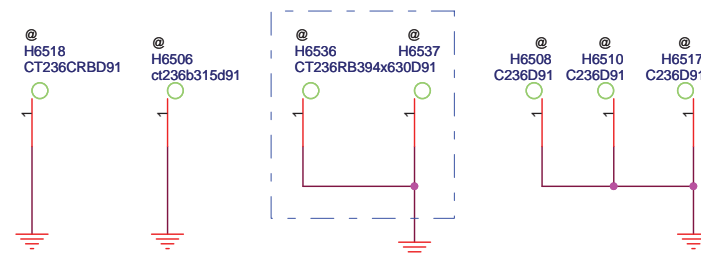
For Fan Stand Off  
C217B189D142 PTH (mirror/BOT)

For KB Stand Off  
CT217B189D142 PTH (TOP)

For MLB Stand Off  
CT217B236I162D142 PTH (BOT)

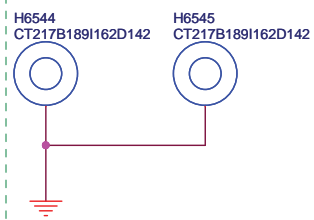


**MLB SCREW HOLE PTH**



For HDD StandOff  
(BOT)

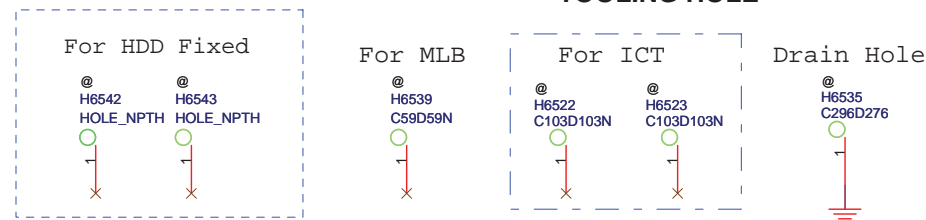
For BT StandOff  
(TOP) 5.5 PAD



H6546  
ROCKY50

R2.1

**TOOLING HOLE**



<b>PEGATRON</b>		Title MDC NUT & Hinksink NUT	
		Engineer: Tina Lee	
Size Custom	Project Name <b>Rocky 40/50</b>		Rev 1.0
Date: Monday, March 24, 2008		Sheet 65	of 94

PEGATRON			Title : E-SATA		
			Engineer: Tina Lee		
Size		Project Name			Rev
A4		Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	66	of 94

5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title :Minicard card & Nut	
		Engineer: Tina Lee	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date: Friday, March 14, 2008	Sheet	67	of 94

5	4	3	2	1
D				
C				
B				
A				

PEGATRON			Title : XDP	
			Engineer: Tina Lee	
Size	Project Name			Rev
A4	Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	68 of 94





5	4	3	2	1
D				
C				
B				
A				

PEGATRON

Title : \*

Engineer: Tina Lee

Size A4	Project Name Rocky 40/50	Rev 1.0
Date: Friday, March 14, 2008		Sheet 70 of 94

5	4	3	2	1
D				
C				
B				
A				

PEGATRON			Title : *		
Engineer: Tina Lee					
Size	Project Name				Rev
A4	Rocky 40/50				1.0
Date: Friday, March 14, 2008			Sheet	71	of 94

5	4	3	2	1
D				
C				
B				
A				

PEGATRON			Title : *	
			Engineer: Tina Lee	
Size	Project Name			Rev
A4	Rocky 40/50			1.0
Date: Friday, March 14, 2008			Sheet	72 of 94

5	4	3	2	1
D				D
C				C
B				B
A				A

PEGATRON

Title : \*

Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date:	Friday, March 14, 2008	Sheet 73 of 94

5	4	3	2	1
D				D
C				C
B				B
A				A

PEGATRON

Title : \*

Engineer: Tina Lee

Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 74	of 94

5	4	3	2	1
D				
C				
B				
A				

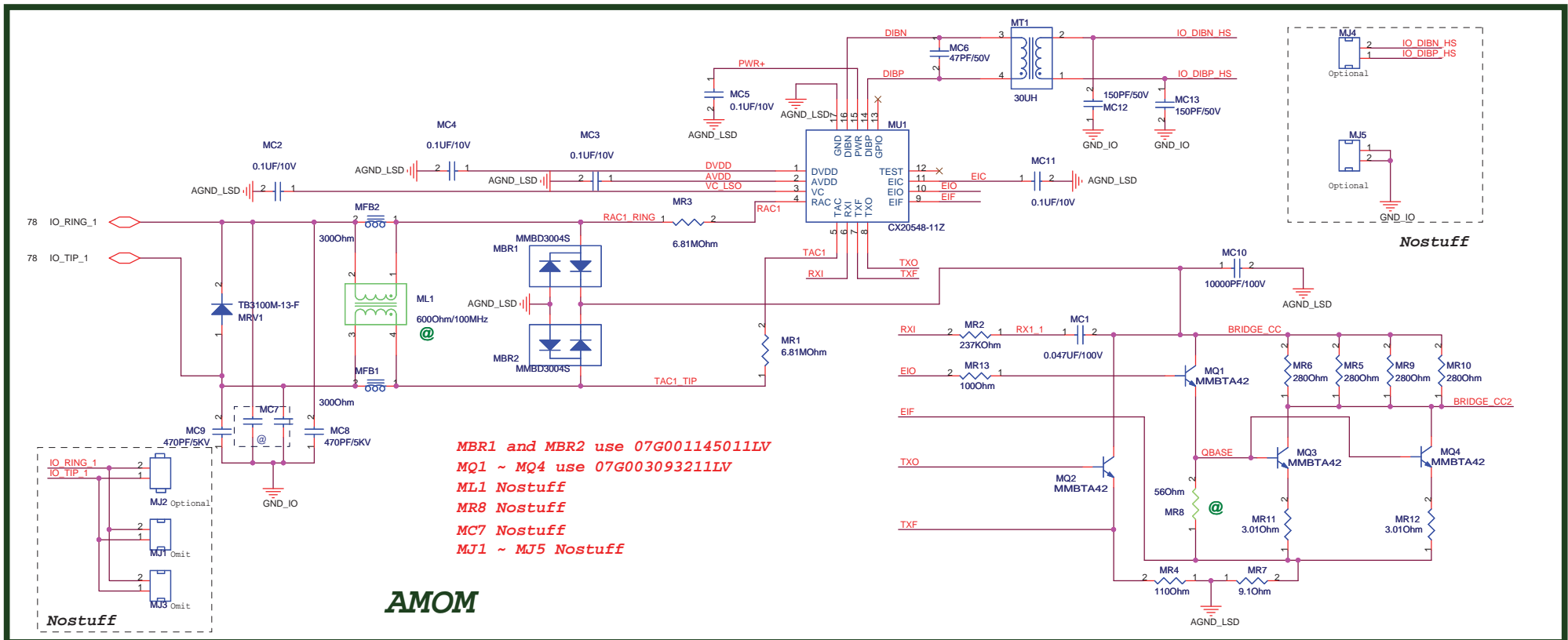
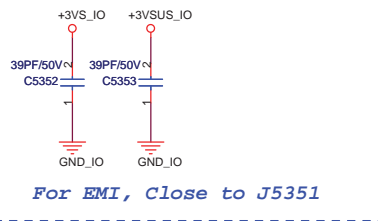
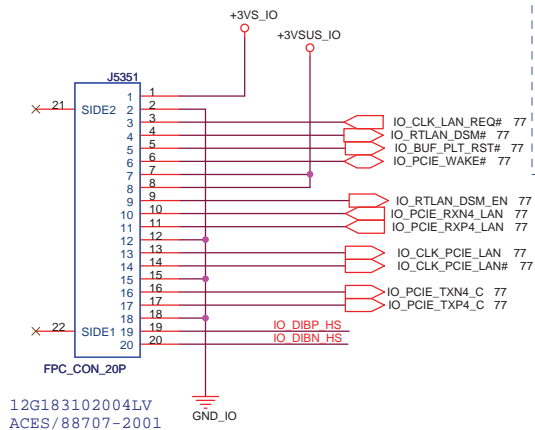
PEGATRON

Title : \*

Engineer: Tina Lee

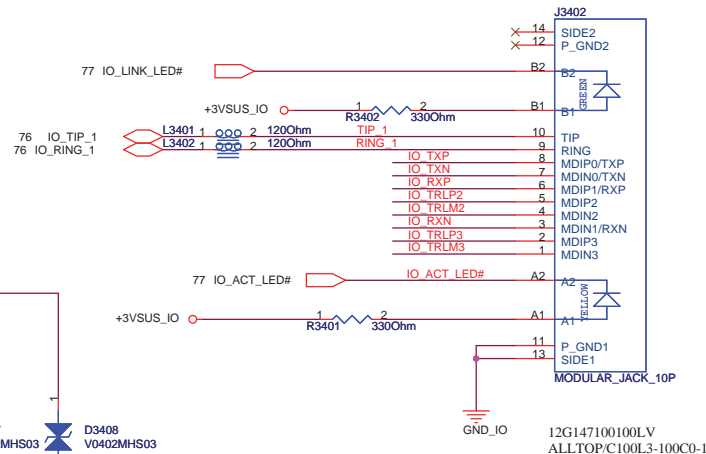
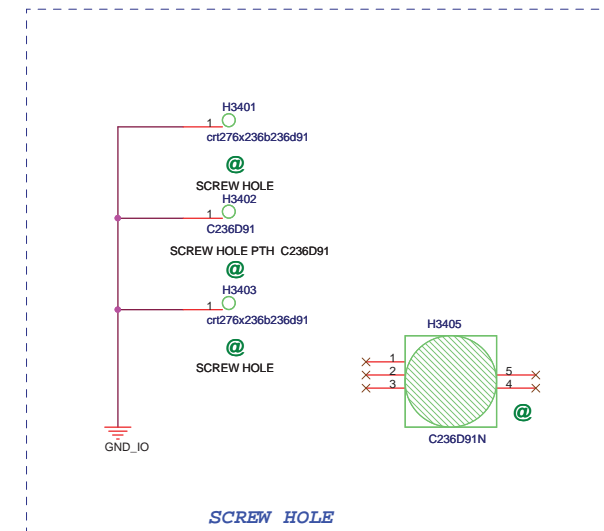
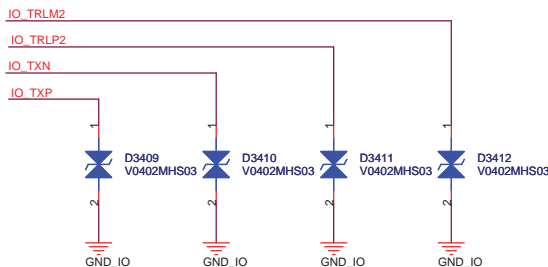
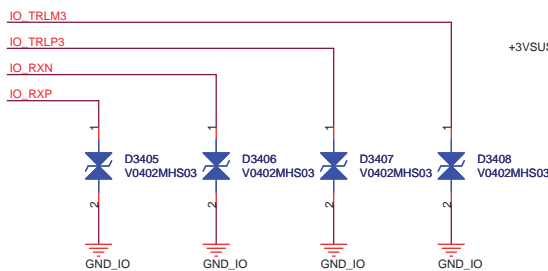
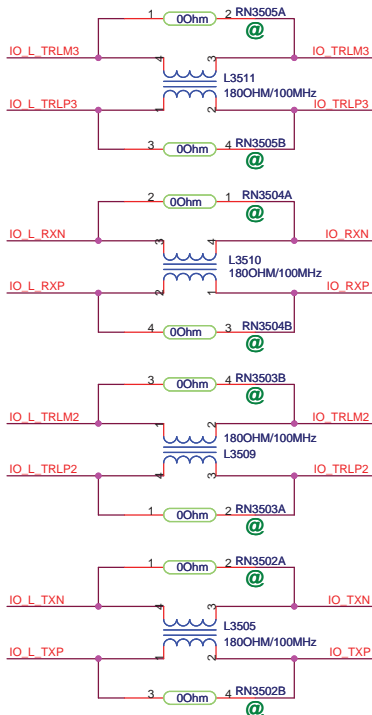
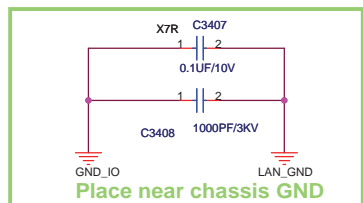
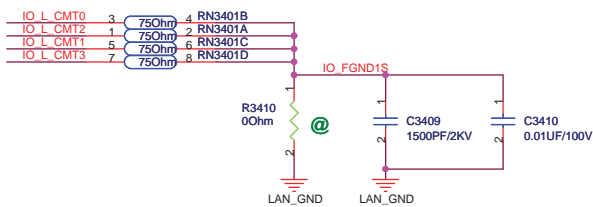
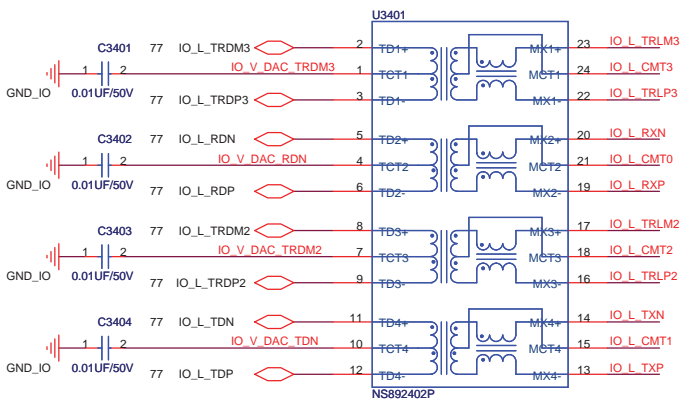
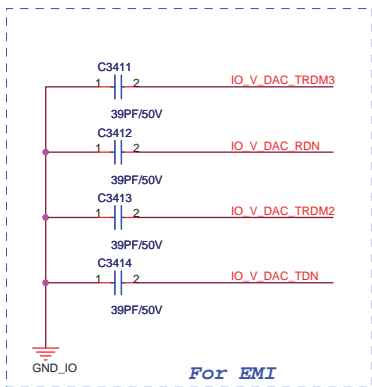
Size	Project Name	Rev
A4	Rocky 40/50	1.0
Date: Friday, March 14, 2008	Sheet 75 of 94	

# IO BOARD







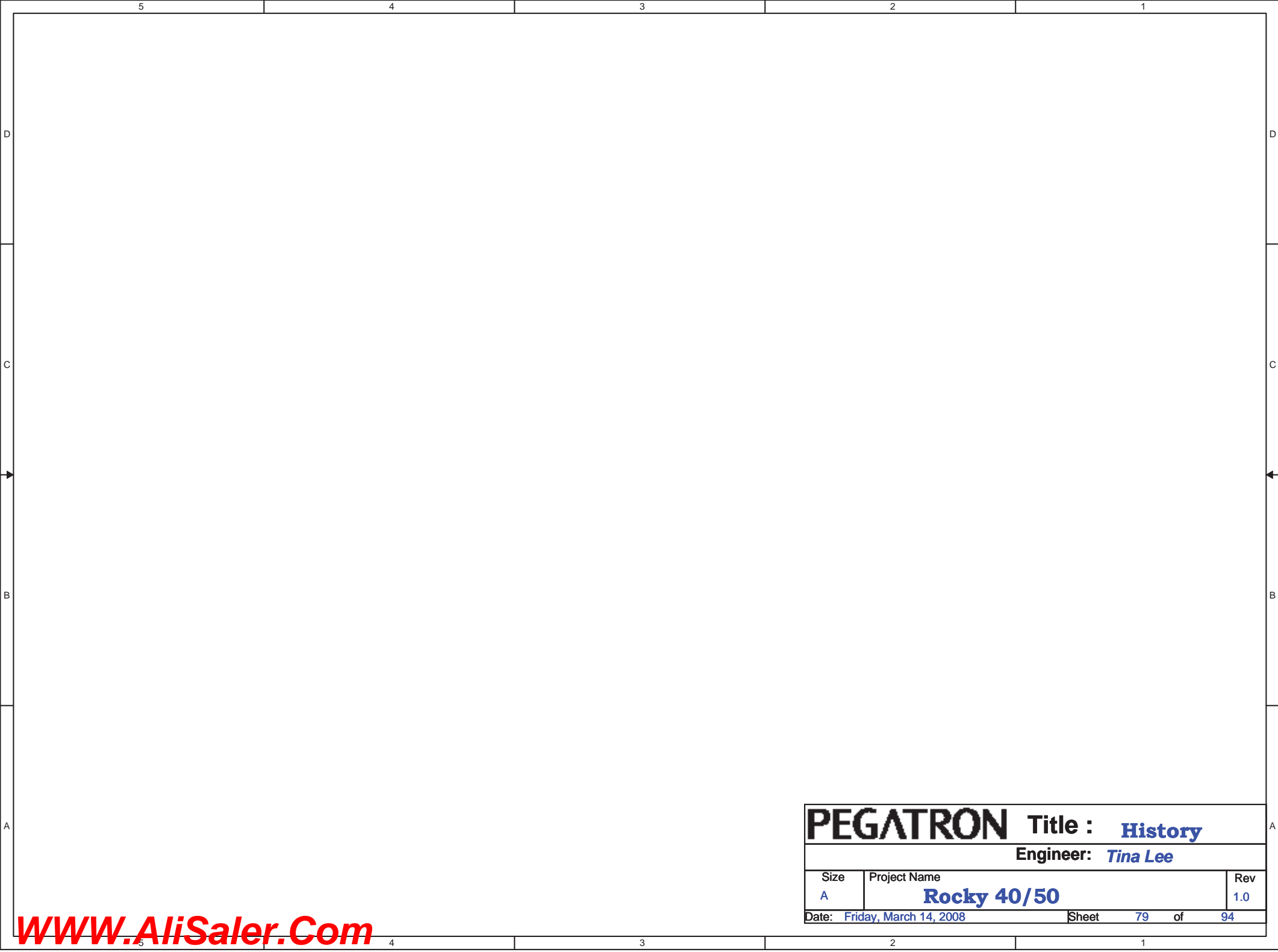


<Variant Name>

ASUS		Title : LAN-RJ45	
ASUSTeK COMPUTER INC		Engineer: Warren	
Size	Project Name	Rocky 50 IO Board	Rev
Custom			2.0
Date: Thursday, March 27, 2008		Sheet 78 of 94	

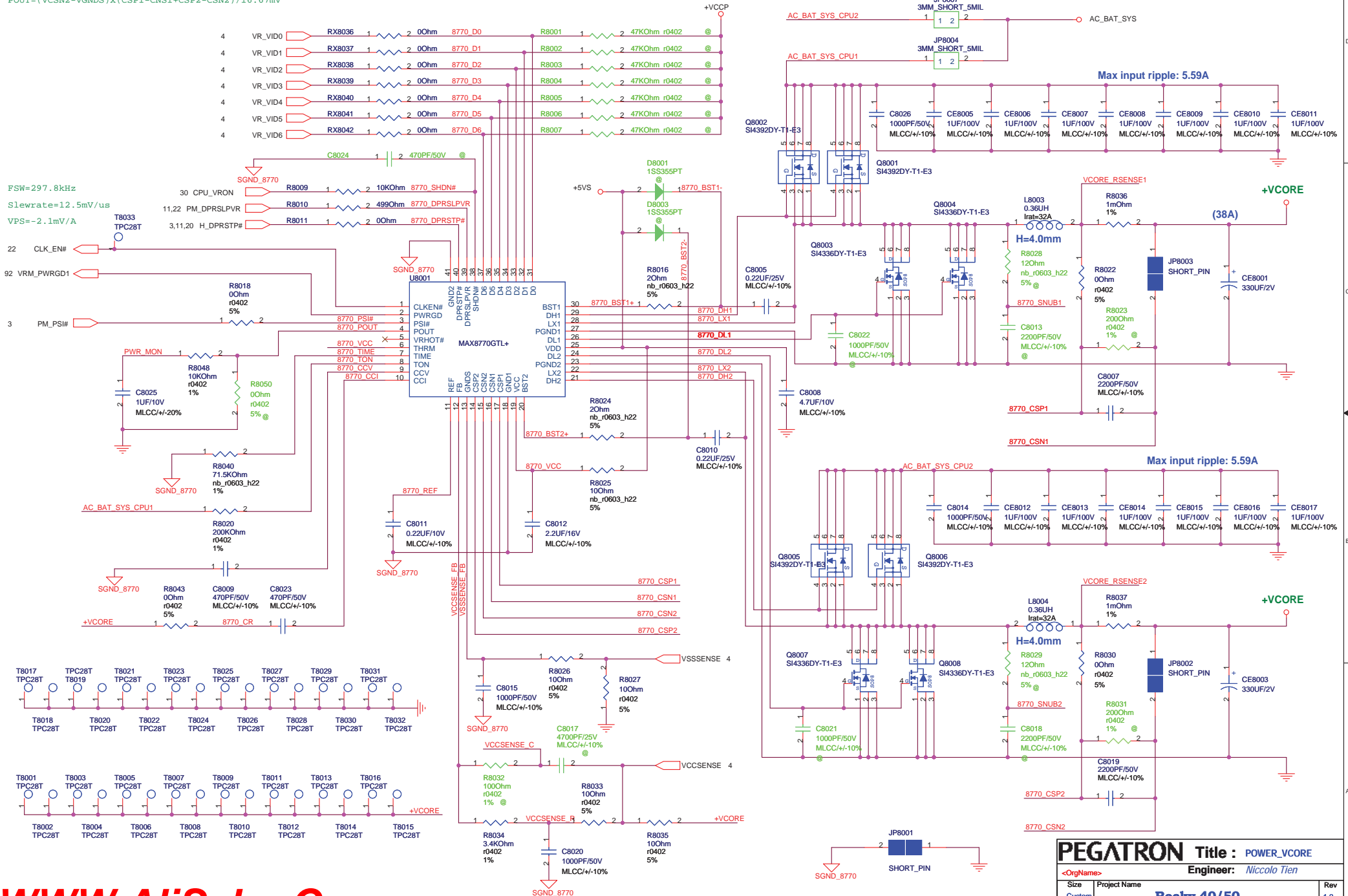


12G147100100LV  
ALLTOP/C100L3-100C0-1



<b>PEGATRON</b>		Title : <b>History</b>	
Engineer: <b>Tina Lee</b>			
Size <b>A</b>	Project Name <b>Rocky 40/50</b>		Rev <b>1.0</b>
Date: <b>Friday, March 14, 2008</b>		Sheet <b>79</b>	of <b>94</b>

```
3.3V level logic level: DPRSLPVR, SHDN#
1.05V level logic: VID, PSI#, DPRSTP#
POUT=(VCSN2-VGNDS)x(CSP1-CNS1+CSP2-CSN2)/16.67mV
```

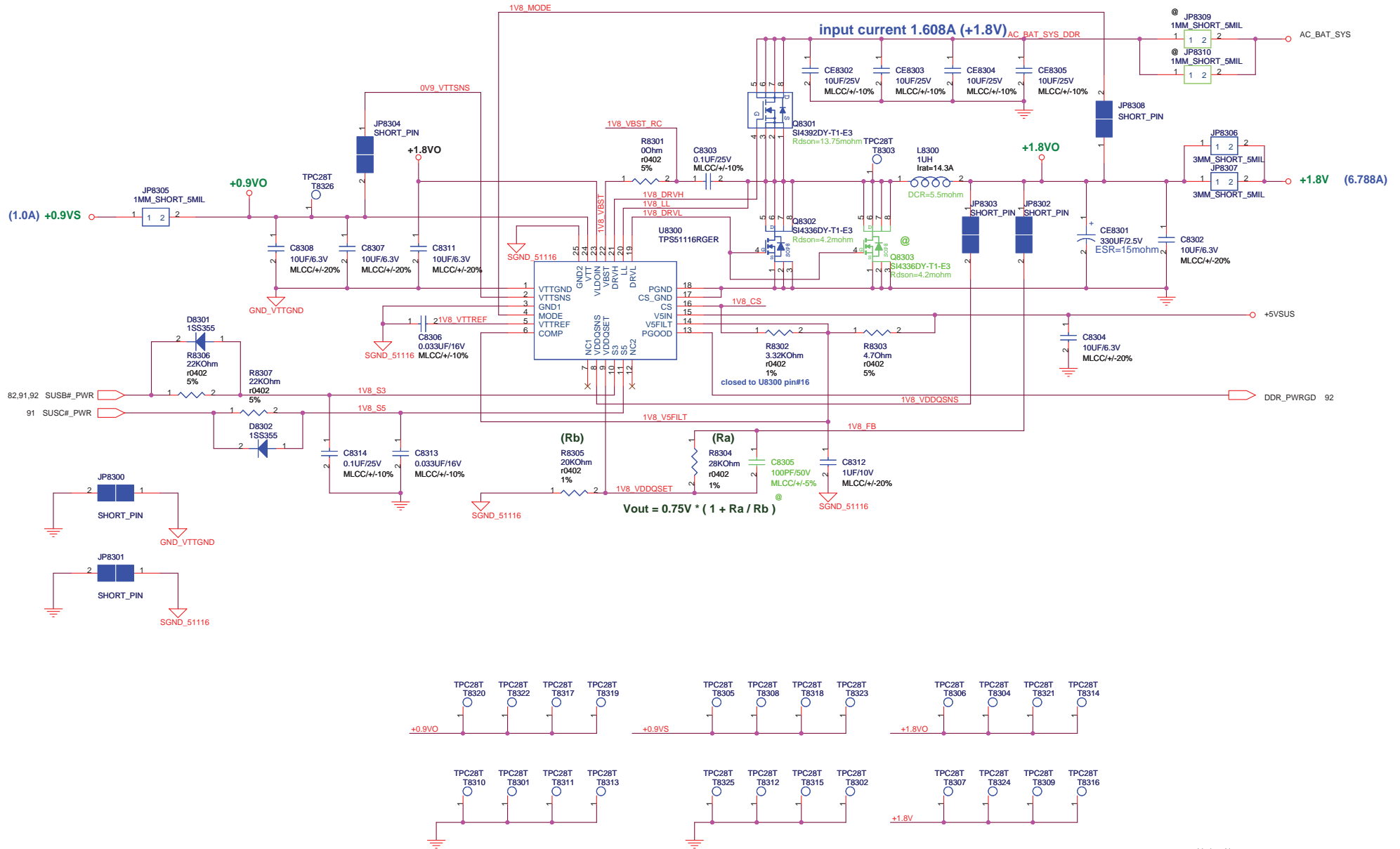


# +5V / +3.3V POWER SUPPLY

(TONSEL = FLOAT, 1.5V = 360KHz /  
1.05V = 300KHz)



# +1.8V / +0.9VS POWER SUPPLY



<Variant Name>

<b>PEGATRON</b>		<b>Title : POWER_I/O_DDR &amp; VTT</b>	
<OrgName>		Engineer: <b>Morris Tseng</b>	
Size Custom	Project Name  <b>Rocky 40/50</b>		Rev 1.0
Date: <b>Thursday, March 27, 2008</b>		Sheet <b>83</b>	of <b>94</b>

5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : PWR_-****	
<OrgName>		Engineer:	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date:	Friday, March 14, 2008	Sheet	84 of 94





PEGATRON		Title :	
<OrigName>		Engineer: <i>Niccolo Tien</i>	
Size	Project Name		Rev
Custom	Rocky 40/50		1.0
Date: Friday, March 14, 2008	Sheet	85 of	94

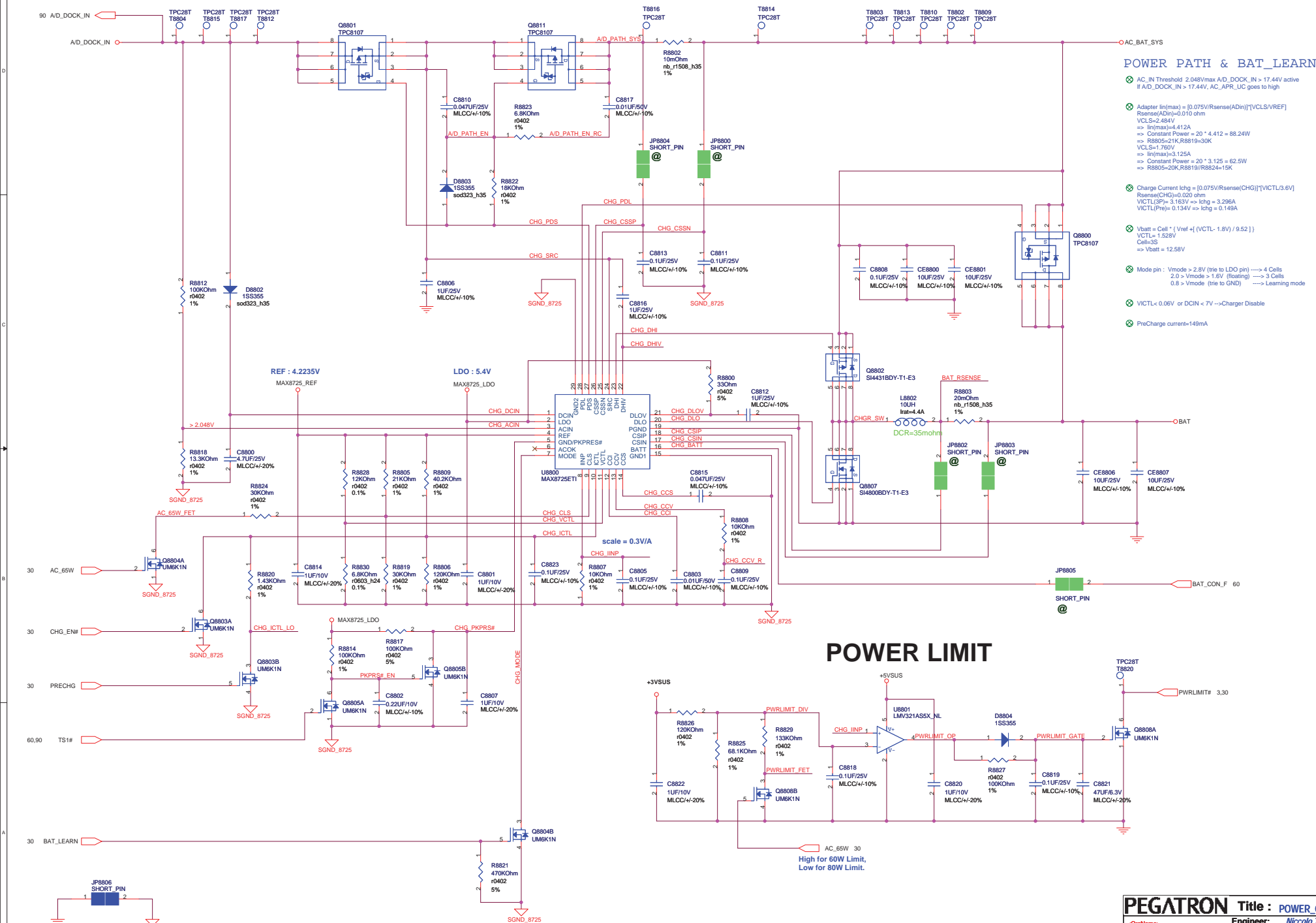
5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : PWR_-****	
<OrgName>		Engineer: Niccolo Tien	
Size A4	Project Name Rocky 40/50		Rev 1.0
Date: Friday, March 14, 2008		Sheet	86 of 94

5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : POWER_SHUTDOWN#	
<OrgName>		Engineer:	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date:	Friday, March 14, 2008	Sheet	87 of 94

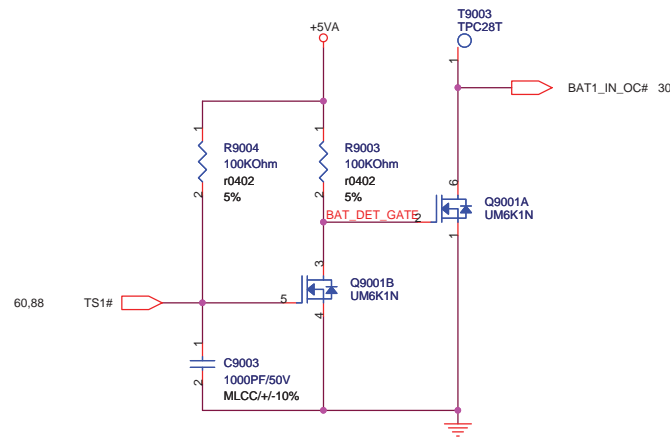
# BATTERY CHARGER



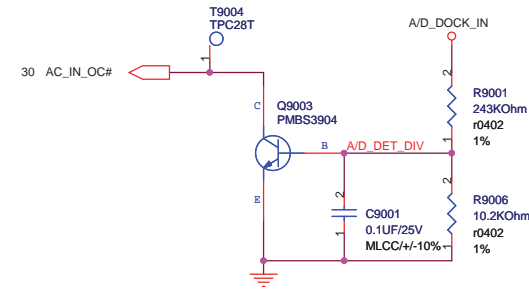
5	4	3	2	1
D				
C				
B				
A				

PEGATRON		Title : TFT-LCD DRIVE	
<OrgName>		Engineer:	
Size	Project Name		Rev
A4	Rocky 40/50		1.0
Date:	Friday, March 14, 2008	Sheet	89 of 94

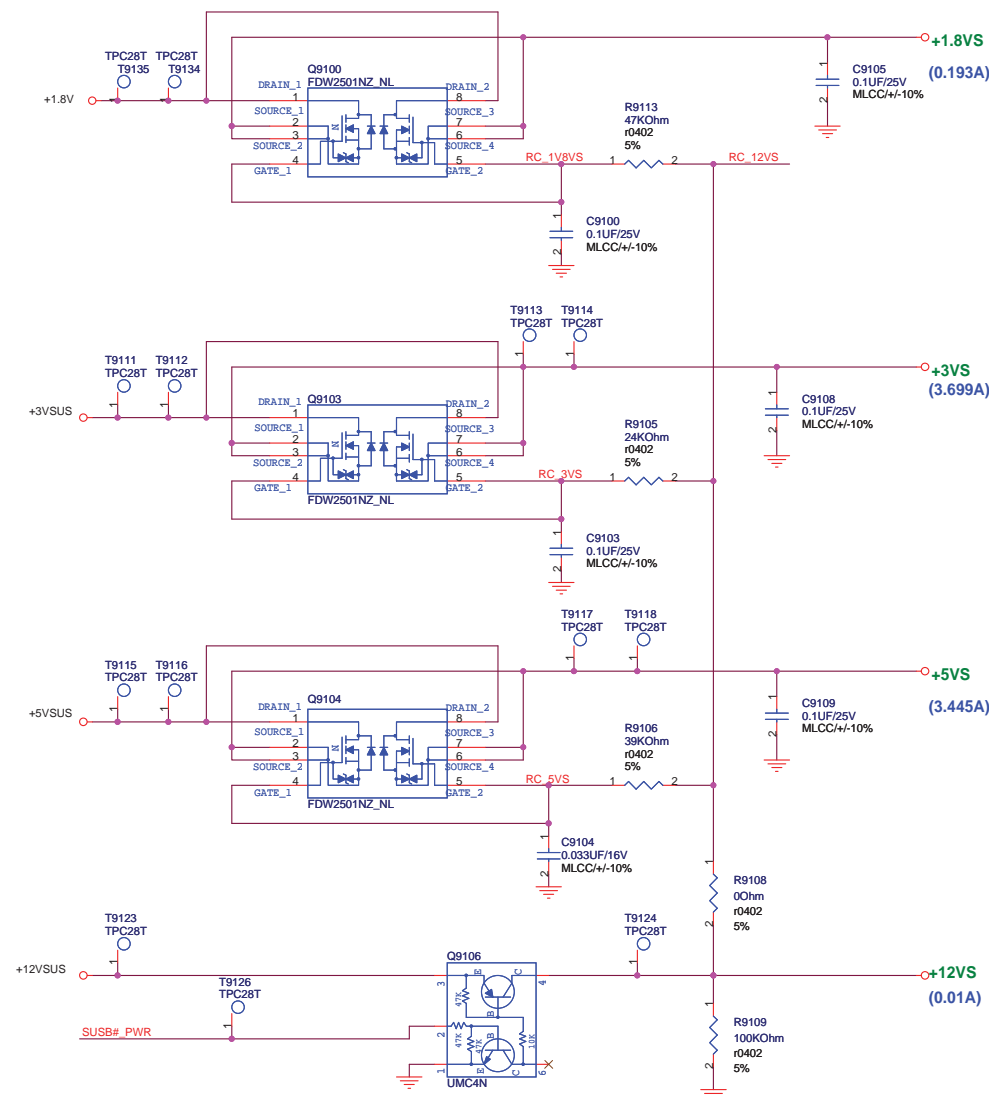
## BATTERY IN DETECT



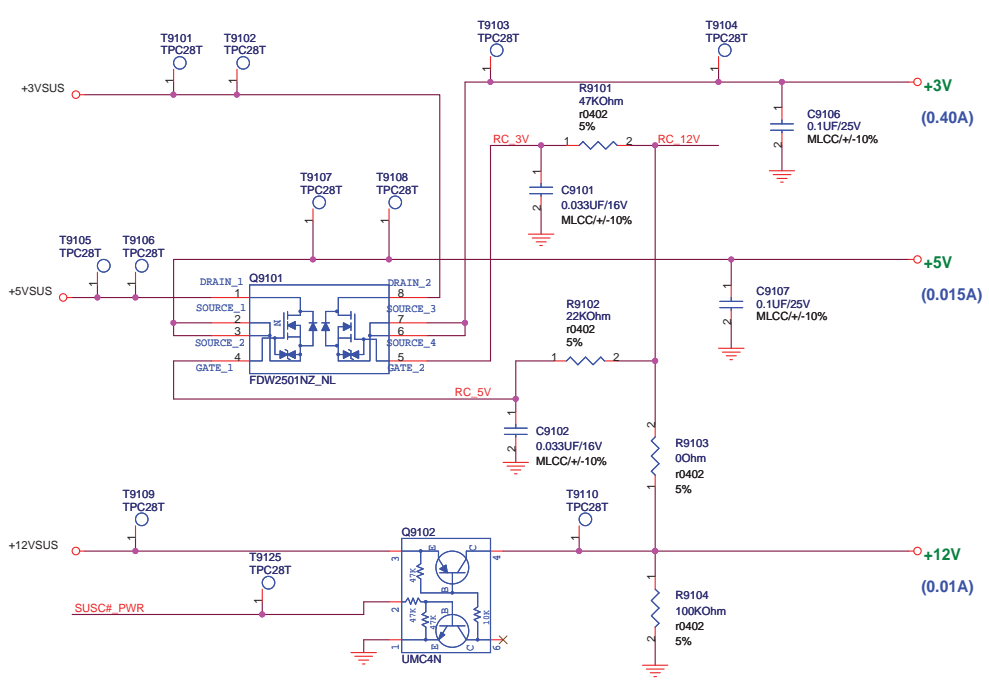
## ADAPTER IN DETECT



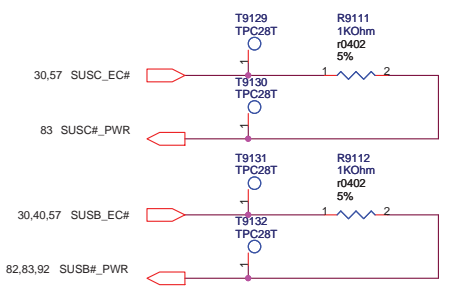
SUSB#\_PWR Load SW



SUSC#\_PWR Load SW



Enable Signal



5	4	3	2	1
---	---	---	---	---

